이학박사 학위논문

4K-bit Microscale Integration and Noise Analysis of Organic Resistive Memory Devices

유기저항변화 메모리에 대한 4K-비트 마이크로 스케일 고집적화와 전기 노이즈 분석

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송영걸의 이학박사 학위논문을 인준함

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Abstract

4K-bit Microscale Integration and Noise Analysis of Organic Resistive Memory Devices

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Organic resistive memory devices have received significant attention for their robust stability, nice performance, solution processable fabrication and flexibility. Employing these advantages, our research group have demonstrated various applications and developments for the organic resistive memory devices such as 1D-1R organic memory devices, vertically stacked memory devices and flexible organic memory devices. However, the high integration of organic resistive memory devices have hardly been demonstrated because it is hard to apply the common photolithography to the organic memory fabrication. Furthermore, because of highly disordered polymer and inhomogeneous composite structure, the switching mechanism of the organic resistive memory devices have not been elaborated understood. In this regard, using the fluorinated photoresist materials and noise analysis method, I studied the highly integrated and microscale organic resistive memory and the switching mechanism in this thesis.

I demonstrated 4K-bit microscale organic nonvolatile resistive memory devices fabricated with a $10 \times 10\ \mu m^2$ cell size in a 64×64 cross-bar array structure. This microscale integration was made via orthogonal photolithography processes using

fluorinated photoresist and solvents and was achieved without causing damage to the underlying organic memory materials. The microscale organic devices exhibited excellent memory performance that was retained more than 10 days with a high ON/OFF ratio (> 10^7) and good endurance switching characteristics (> 300 cycles). The demonstration of 4K-bit organic memory devices promises a possibility of highly-integrated microscale organic electronics applications. Furthermore, I presented the integration of flexible and microscale organic nonvolatile resistive memory devices fabricated in a cross-bar array structure on plastic substrates.

The origin of negative differential resistance (NDR) and its derivative intermediate resistive states (IRSs) of nanocomposite memory systems have not been clearly analyzed. To address this issue, the current fluctuations were investigated over a bias range that covers various intermediate resistive states and negative differential resistance (NDR) in organic nanocomposite unipolar resistive memory devices. From the analysis of the $1/f^{\gamma}$ type noises, scaling behavior between the relative noise power spectral density $\tilde{S}$ and resistance R was observed, indicating a percolating behavior. I investigated the current fluctuations of organic nanocomposite memory devices with NDR and the IRSs under various temperature conditions. The $1/f$ noise scaling behaviors at various temperature conditions in the IRSs and telegraphic noise in NDR indicated the localized current pathways in the organic nanocomposite layers for each IRS. The clearly observed telegraphic noise with a long characteristic time in NDR at low temperature indicated that the localized current pathways for the IRSs were attributed to trapping/de-trapping at the deep trap levels in NDR. This study will be useful for

the development and tuning of multi-bit storable organic nanocomposite memory device systems.

Keywords : Organic resistive memory, Orthogonal photolithography, 1/f noise, Random telegraph noise, Percolation
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Chapter 1. Background Knowledge

1.1. Organic resistive memory devices

In the last decade, resistive memory have been attracted great interest from both industrial and academic researchers. Resistive memory devices, which have two-terminal structure, change their resistance by modulating the applied voltage. In succession to the success of oxide-based inorganic resistive memory devices regarding fast data storage speed, high data storage integration capability (cross-bar architecture), and stable storage endurance, resistive memory devices are possibly considered to be a next generation next to flash memory devices [1]. Along the development of the oxide-based resistive memory devices, organic memory devices have taken attention from many researchers due to low cost, ease of fabrication, large-area processibility, material variety, flexibility and printability of organic-based materials. There are several kinds of structures for the organic resistive memory devices such as single layer, bilayer, semiconducting or conducting nano-layer embedded in organic matix, and nanocomposite layer where semiconducting or conducting nanoclusters are embedded and distributed in organic matrix. Among them, I have focused on fabrication and development of organic nanocomposite resistive memory devices (ONRM) for their excellent device performance, and extremely simple fabrication process. ONRM usually exhibits unipolar switching property, in which the switching on and off of the memory occurs in same voltage direction and the switching operation can be possible both positive and negative bias. Furthermore, ONRM also exhibits the

multi-level current states, which enables the multibit storage of information and neuromorphic application. Using ONRM, our research group have developed significant applications such as 1D-1R organic memory devices, vertically stacked organic memory devices and flexible organic memory devices.

1.2. Orthogonal photolithography

Organic resistive memory devices are hard to be fabricated in microscale because common photolithography cannot be applied to them. Especially, usage of acetone in lift-off process can severely damage the organic layer because most organic materials are miscible to acetone. Regarding this, highly fluorinated chemicals were extensively studied to be applied as a new photolithography method. Because fluorinated chemicals are orthogonal to oleophilic or hydrophilic organic materials, they can be used as photoresist materials for fabrication of microscale organic electronic devices. Recently, semi-perfluoroalkyl resorcinarene (denoted as R_F-Calix-tBoc) have been used as photoresist material to apply photolithography on organic electronic devices [2,3]. The solvents for development and lift-off are HFE 7500 and HFE 7200, which are highly fluorinated solvents and eco-friendly property. R_F-Calix-tBoc is blended with photo acid generator in HFE 7500 with small amount of propylene glycol methyl ether acetate (PGMEA). If this fluorinated photoresist is spun coated on a substrate and exposed to UV light, acid-catalyzed deprotection reaction leads to the film to be highly polar because of hydroxyl group formation (Fig. 1.1). So that the resist film cannot be soluble in HFE 7200, while screened film is soluble in HFE 7200. This enables the photolithography using R_F-Calix-tBoc in negative tone.

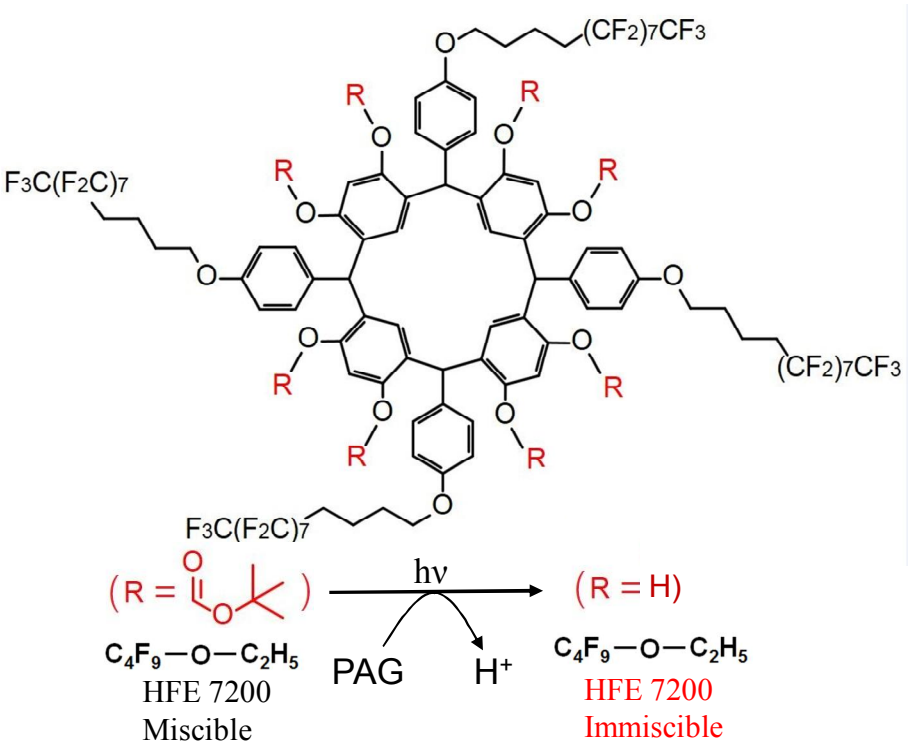


Figure 1.1 Chemical structure changes when our fluorinated photoresist (Semi-perfluoroalkyl resorcinarene) is exposed to UV light.

1.3. Noise sources in organic electronic devices

The noise in electronic devices is usually measured by biasing the current or voltage of the device. If a device is biased using the voltage, one can measure the current noise and vice versa. The fluctuation in the current and voltage response in the time domain can be sampled using a specific time interval. Let us denote the fluctuation in the voltage, current or resistance recorded in time as *X(t)*, which by

itself can provide useful information if it shows random telegraph noise in which a number of stable current levels exist. However, in most cases, *X(t)* is the result of the superposition of various noise signals, such as flicker noise, thermal noise, shot noise, and Lorentzian noise. Therefore, it is more useful to investigate the noise spectra by decomposing each frequency component from *X(t)*. With this requirement, estimating the power spectral density is the most preferable way to analyze the noise data. To estimate the power spectral density, one needs to calculate the autocorrelation function ($A(\tau)$) of *X(t)* [4].

$$A(\tau) = \langle X(t+\tau)X(t)\rangle \tag{1.1}$$

Then, the Fourier transform of the autocorrelation function multiplied by two results in the power spectral density ($S_X(f)$).

$$S_X(f) = 2\int_{-\infty}^{\infty} d\tau\, e^{i\omega\tau} A(\tau) \tag{1.2}$$

This relation between the power spectral density and time series is mathematically well defined and is called the Wiener-Khintchine theorem. The autocorrelation function determines the correlation between two data points with an interval of τ, revealing the characteristics of the noise process. For example, for white noise, $A(\tau) = \delta(\tau)$, showing the constant frequency dependence of $S_X(f)$. The physical meaning of the power spectral density is the frequency component of the noise power average per unit frequency band. The noise power average, which is the mean squared signal of the variance of the fluctuations, can be expressed as the integral of $S_X(f)$ over all the positive frequencies.

$$\langle (\delta X)^2 \rangle = \int_0^{\infty} df\, S_X(f) \tag{1.3}$$

Noise spectra in electronic devices are classified into several types according to

their noise sources or frequency dependence. There are four types of important noise in this review: thermal noise, shot noise, random telegraph noise, and *1/f* noise. Table 1 summarizes the noise types reported in the OEDs.

Table 1 Noise types observed from organic electronic devices

Noise type	Noise source	Devices	Power spectral density
Thermal noise	- Thermally induced motions of charge carriers	- Any resistor	
Shot noise	- Discrete nature of charge carriers - Random arrival of charge carriers at the channel	- Single-molecule junctions	
Random telegraph noise	- Trap/detrap of charge carriers at the trap center	- Metal-oxide polymer resistive memory - Organic nanocomposite resistive memory - SAM junctions	
	- Conformational change of molecules	- Single-molecule junctions	
1/f noise	- Explicit source is unknown	- Organic thin film transistors - Metal-oxide polymer resistive memory - Organic nanocomposite resistive memory - SAM junctions - Single-molecule junctions	

1.3.1. Thermal Noise

The thermal motion of charge carriers can cause random fluctuations in the current, which is called thermal noise (Johnson-Nyquist noise) [4]. The thermal noise is only determined by the dissipative nature of the conductor (resistance (R) and temperature (T)), which can be derived from the fluctuation-dissipation theorem (this is why the thermal noise is called equilibrium noise). The expression for the thermal noise is frequency independent in the quasi-classical regime ($hf << k_BT$) [4]:

$$S_V = 4k_BTR; S_I = 4k_BT/R \quad (1.4)$$

where S_V is the voltage noise power spectral density, S_I is the current noise power spectral density and k_B is the Boltzmann constant. The thermal noise shows white

noise (constant power spectral density) under usual experimental conditions (for example, the quasi-classical regime holds up to 10^{11} Hz at 4 K). Because the thermal noise is not affected by the microscopic structure of the organic material and is only affected by R and T, the thermal noise itself may not be considered to be an interesting topic in organic electronics. However, one should carefully consider the thermal noise during noise measurements because the thermal noise can hinder the noise of interest within a certain range of the frequency band.

1.3.2. *1/f* Noise

Specified by its name, any electronic noise that exhibits a power spectrum density with a $1/f^{\gamma}$ frequency dependence ($0.9 < \gamma < 1.1$) is called *1/f* noise. This type of noise can be observed in most semiconductor systems, such as MOSFETs [5–7], bipolar junction transistors (BJTs) [8], thin film transistors [9], light emitting diodes [10,11], solar cells [12], magnetic random access memory (MRAM) [13], flash memory [14], and resistive random access memory (RRAM) [15–18]. Because *1/f* noise appears ubiquitously in electronic systems from the bulk size to molecular size and from crystals to disordered systems, a well-defined process or mechanism explaining all the *1/f* noises in various systems does not exist. However, there are a number of insightful explanations that are limited to specific ranges of systems. In the semiconductor physics field, a tremendous number of studies has been conducted since the 1950s regarding the analysis of *1/f* noise in semiconductors [4,19–25]. Here, I introduce representative explanations that will be helpful for understanding this review. In the 1950s, McWhorter suggested that *1/f* noise is caused by charge carrier number fluctuations

at the interface between the semiconductor and oxide [20,25]. In oxides, the traps are distributed uniformly, and charge carriers in the semiconductor can be trapped and detrapped at the oxide traps, causing number fluctuations in the conductive charge carriers. These fluctuations are called generation-recombination (GR) noise and exhibit a Lorentzian spectrum for a single trap. Because there are a number of traps inside the oxide, the resultant noise is the superposition of the GR noises with different characteristic times for each trap. If the traps are distributed uniformly in the oxide and electrons can be trapped due to tunneling, the distribution of the characteristic times is proportional to $1/\tau$. For the distribution in the range of τ_1 and τ_2, *1/f* noise can occur in the range of $\tau_1 < \tau < \tau_2$ due to the superposition of the GR noises. McWhorter's description provides a very useful framework for understanding *1/f* noise, so the description has been employed for describing the noise in various FET systems.

In 1960s, Hooge proposed a universal empirical relation from a number of noise measurements in metal and semiconductors, which is called Hooge's empirical relation [20,21,26,27].

$$\frac{S_R}{R^2} = \frac{S_I}{I^2} = \frac{S_V}{V^2} = \frac{\alpha}{f N_c} \tag{1.5}$$

where α is called the Hooge parameter and N_c is the total number of free charge carriers inside the material. The relation describes the bulk noise inside a specimen, as indicated by N_c. Initially, α was found to be approximately 2×10^{-3} for ohmic homogeneous samples, and it was considered to be a universal constant. However, in later studies, α was found to be dependent on the temperature, magnetic field, crystallinity, and material type. Therefore, Hooge's relation is not a universal relation, although the relation can be considered as a useful standard for noise

experiments. In homogeneous and ohmic samples, the measured α value does not deviate by more than two orders of magnitude from 2×10^{-3}. Strongly disordered and inhomogeneous samples can have many orders higher than 2×10^{-3}, as the effective number of free charge carriers may be much smaller than N_c. In organic semiconductor devices, all α values have been measured to be higher than 2×10^{-3}, depending on the material type and device structure. Based on Hooge's empirical relation, the bulk mobility fluctuation induced by charge scattering has been considered to result in *1/f* noise [28].

In 1990s, researchers tried to explain *1/f* noise in MOSFET devices as the contribution of both number fluctuations and mobility fluctuations [29,30]. The fluctuations in the oxide trap occupancy can affect the scattering rates and cross sections of the charge carriers in a semiconductor and are referred to as correlated fluctuations between the carrier number and surface mobility. One of the most widely used noise relations for correlated fluctuations was proposed by Ghibaudo et al. and is expressed as [29]

$$\frac{S_I}{I^2} = \left(1 + \alpha_{sc}\mu_{eff}C_{ox}\frac{I_{SD}}{g_m}\right)^2 \frac{g_m^2}{I_d^2} S_{fb} \tag{1.6}$$

where α_{sc} is the scattering coefficient, μ_{eff} is the effective mobility, I_{SD} is the source-drain current, C_{ox} is the gate oxide capacitance, g_m is the gate transconductance and S_{fb} is the flat band voltage spectral density. Note that this relation cannot explain the origin of *1/f* noise; however, one can inspect the dependence of the noise on I_D and g_m and then check the degree of the noise correlations with the gate oxide charge trapping fluctuations.

In organic electronic devices, *1/f* noises have been found in almost all the devices, and they depend on the gate voltage, luminescence, voltage bias regime,

resistance, and microscopic structure. Although 1/f noises in disordered organic materials are hard to explain, analyzing their dependence on various factors has provided meaningful insights into the charge transport mechanisms and microscopic structures of organic materials.

1.3.3. Random telegraph noise

Random telegraph noise (RTN) indicates an electronic noise in which discrete random transitions appear between two or more voltage/current levels. RTN has been observed in various electronic systems, such as metal-oxide-semiconductor field effect transistors (MOSFETs) [30–32], resistive memory devices [15,33,34], point contacts [35], and nanogap junctions [36,37]. Generally, RTN is known to be generated by the contribution of thermally activated transitions or tunnel transitions between energy wells [38]. In the case of the two-level RTN observed in MOSFETs, it is well known that the charge trapping/detrapping at a single trap inside the oxide layer is responsible for the RTN [4,39,40]. In oxide-based resistive memory devices, RTN has been reported for various resistance states and has usually been attributed to the traps distributed in the oxide memory material [41–43]. With the exponential decay of $A(\tau)$ ($\sim exp(-\tau/\tau_0)$, where τ_0 is the relaxation time of the random telegraph noise), two-level RTN is known to exhibit a Lorentzian power spectral density [4]

$$S_I \propto \frac{1}{1+(2\pi f \tau_o)^2} \tag{1.7}$$

However, the power spectral density cannot provide all the useful information regarding RTN because alterations in the conductance states and the amplitude levels between the states cannot be clearly deduced from the power spectra.

Therefore, when analyzing RTN, time domain measurements and their direct statistical analyses are important for understanding the physical nature of the system. For example, the mean spent time (τ_2 and τ_1) in each state of two-level RTN is usually found to have an exponential relation with the inverse temperature ($1/T$) [4,32,44]:

$$\tau_1 \propto \exp\left(\frac{E_1}{k_B T}\right), \tau_2 \propto \exp\left(\frac{E_2}{k_B T}\right) \quad (1.8)$$

where E_1 and E_2 are the activation energies of each state. In organic electronic devices, RTN has been observed in organic resistive memory devices, SAM junctions, and single-molecule junctions due to contributions from the traps or conformation changes in the molecules.

Chapter 2. High integration of organic resistive memory devices.

2.1. Introduction

Organic material-based devices have recently received significant attention for their various advantages, including low manufacturing cost, large area processing capabilities, flexibility, and printing processes [45–50]. Due to these advantages, researchers have investigated a wide range of possible applications for these new devices, such as organic field effect transistors, organic light-emitting diodes, organic photovoltaic cells, organic sensors, and organic memories [47–53]. In particular, organic nonvolatile memory is considered to be a promising candidate for information storage devices because of its ease of fabrication, good performance, and durability [1,53–57]. Organic memory devices have often been fabricated in a cross-bar structure, which can realize high integration of memory cells [1,54–64].

However, the cross-bar structured organic memory devices have usually been limited to be less than a hundred bits integration with the individual cell size of several hundreds of microns (μm). The conventional photolithographic patterning technique to scale down the devices is difficult to apply to organic electronics because of the chemical incompatibility between organic electronic materials and organic solvents for photolithographic processing. Organic solvents (e.g., the developer used in lithography or acetone) dissolve not only the photoresist but also

the organic electronic materials. Because of this issue, the majority of previous studies on organic electronic devices, including organic memory devices, have been restricted to non-lithographic fabrication methods, such as processes employing shadow masks or imprints. This lithographic problem makes it difficult to integrate organic memory devices into a smaller device size at the micrometer scale. Other fabrication techniques for manufacturing organic memory devices that might overcome the scale-down problems have been studied, including nanowire pattern transfer, the direct metal-transfer method, and a method using photo cross-linkable organic memory [64,65]. However, because of their complicated processes, these methods may not be practical for high throughput, low-cost fabrication of delicate device structure, application to various memory materials and high integration of organic memory devices. For example, contact-based printing methods such as nanowire pattern transfer and direct metal-transfer method require a perfectly flat morphology in the bottom electrodes to prevent the disconnection of the transferred top metal lines. Application of photo cross-linkable organic memory is also limited to its crosslinking polymers due to its use of acetone.

To overcome the lithographic problem in organic electronics, some groups, including ours, have demonstrated a chemically non-damaging orthogonal photolithographic method that allows us to protect the underlying polymer organic films from the action of lithographic chemicals [2,3,66,67]. One possible solution is to use fluorinated photoresist (such as semi-perfluoroalkyl resorcinarene) and solvents (such as hydrofluoroethers) which are miscible to each other and orthogonal to most organic materials. These materials allow organic electronic devices to be fabricated at the microscale using the photolithography process [2,66].

In this study, I demonstrate the microfabrication of highly-integrated 4K-bit (64 × 64 array) organic nonvolatile resistive memory devices with a 10 × 10 μm^2 cell size, made possible by using fluorinated photoresist and solvents to avoid damaging the underlying organic memory materials. The fabricated organic memory devices exhibited a high ON/OFF ratio, stable switching characteristics, and excellent durability in terms of retention and endurance characteristics. Our devices showed a desirable operational uniformity and high device yield of operative memory distribution over the 4K-bit integration of organic memory devices.

2.2. 4K-bit and microscale integration

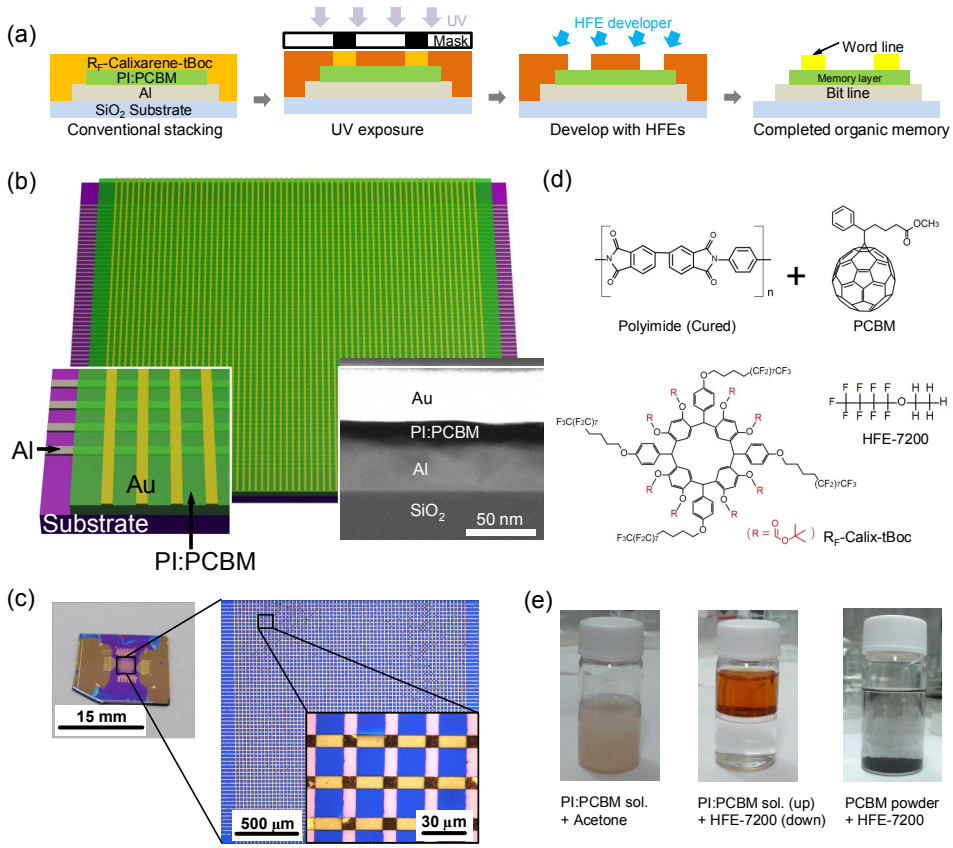


Figure 2.1 Experimental preparation for application of orthogonal photolithography on organic resistive memory. (a) Schematics illustrating the microscale organic memory devices. (b) Schematic of the 4K-bit nonvolatile resistive organic memory devices on a Si substrate with a zoomed-in schematic (left bottom inset). Right bottom inset shows a cross-sectional TEM image of an organic memory cell. (c) Optical images of the fabricated 4K-bit organic memory devices. The line width of the electrodes is 10 μm. (d) Chemical structures of cured PI and PCBM used as the memory material together with those of semi-perfluoroalkyl resorcinarene and HFE-7200 used as the photoresist and developer, respectively. (e) Optical images of (left) the mixed solution of PI:PCBM and acetone, (middle) two phase-separated solutions of PI:PCBM and HFE-7200, and (right) PCBM powders, which sink to the bottom of HFE-7200.

2.2.1. Application of orthogonal photolithography

Figure 2.1(a) illustrates the fabrication process for a 4K-bit microscale organic memory array using the orthogonal photolithographic method. For the fluorinated photoresist solution, 10 wt% of semi-perfluoroalkyl resorcinarene powder and 0.5 wt% of N-nonafluorobutanesulfonyloxy-1,8-naphthalimide photoacid generator were dissolved into a mixed solvent (3-ethoxy-1,1,1,2,3,4,4,5,5,6,6,6-dodecafluoro -2trifluoromethylhexane (HFE-7500):propylene glycol methyl ether acetate (PGMEA) = 4:1 weight ratio), and the solution was filtered through a 0.20-μm nylon syringe filter. For the active memory material (PI:PCBM), 2 ml of BPDA-PPD solution (10 wt% in NMP) and 0.3 ml of PCBM solution (0.5 wt% in NMP) were mixed and then diluted with 11.3 ml of NMP to control the active layer thickness. First, a SiO_2 (270 nm thick)/Si substrate was prepared and cleaned using acetone, isopropanol, and de-ionized water. The 20-nm-thick Al bottom electrode lines with 10 μm line width were fabricated using conventional photolithography. To enhance the film uniformity, the Al bottom electrodes deposited on the SiO_2/Si substrate were exposed to UV-ozone for 10 min [57]. The prepared memory solution was spin coated onto the substrate, followed by soft-baking on a hot plate at 120 °C for 5 min in a N_2-filled glove box. Then the PI:PCBM layer was hard-baked on a hot plate at 300 °C for 30 min. Then, the fluorinated photoresist solution was spin coated, followed by baking process at 75 °C for 3 min under yellow light. Subsequently, the coated photoresist film was exposed under UV light (416 nm wavelength, intensity of ~8 mW/cm^2) through a photomask with 10 μm lines orthogonal to the bottom electrode lines. After post-exposure baking at 75 °C for 3 min, the photoresist film was developed

by HFE-7200. The pattern after the development was highly sensitive to the UV exposure time (Fig. 2.2). If the UV exposure time is short (4 s), the edge of the pattern exhibited wavy shape, narrowing the width of the electrode. If the UV exposure time is long (6 s), there are some residues in the line, indicating that the UV light affected the photoresist under the chrome mask due to the diffraction. Top electrodes of a 30 nm-thick Au layer were deposited on the developed samples. For the 4K-bit organic memory array devices, the sample was lifted off in an ethanol (5 vol%)-HFE-7200 (95 vol%) mixture to leave patterned Au electrodes on top of the PI:PCBM film. Figure 2.1(b) shows the schematics and a cross-sectional transmission electron microscopy (TEM) image (right bottom inset) of the 4K-bit (64 × 64 = 4096 bits) organic memory devices, which were fabricated with Al bottom electrodes and Au top electrodes on a Si substrate in the cross-bar structure. The width of the Al or Au electrodes was 10 μm and the interval between the Al or Au electrodes was 30 μm, which was defined with the microlithography process.

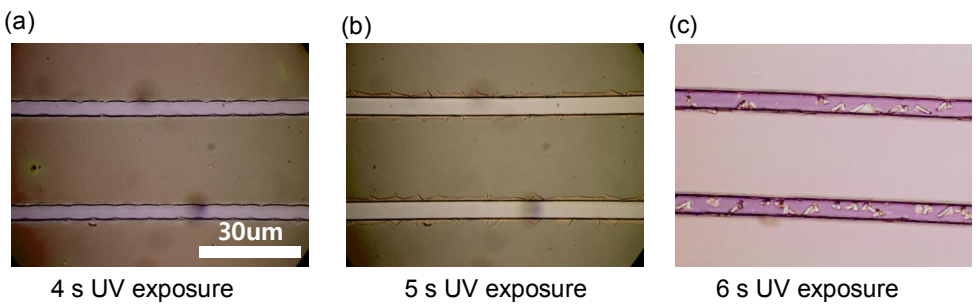


Figure 2.2. Fluorinated resist pattern changes under UV exposure time (a) 4 s, (b) 5 s, (c) 6 s.

A composite of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PCBM) was used as the active memory material due to its mechanical robustness and thermal stability [60–64]. The TEM image in Fig. 2.1(b) indicates the well-separated PI:PCBM active layer (~15 nm thick) between the Al (~25 nm thick) and

Au (~30 nm thick) electrodes. Figure 2.3 shows the cross-sectional analysis of a microscale organic memory device using transmission electron microscopy (TEM) image and energy dispersive x-ray spectroscopy (EDX) mapping method. Top Au elements were well separated from the bottom Al and did not infiltrate into the PI:PCBM layer. With these observations, it is confirmed that the PI:PCBM layer is not damaged by orthogonal photolithography process using fluorinated materials. Also the switching effect is mediated by PCBM molecules in the PI matrix without the effect of inclusion of Au elements.

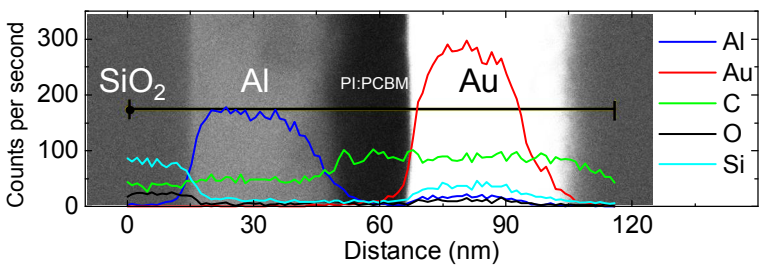


Figure 2.3 Cross-sectional TEM and EDX mapping image for element analysis.

Fig. 2.1(c) shows optical images of the 4K-bit microscale organic memory devices with a memory cell size of 10 × 10 μm^2, which were integrated in a 1.9 × 1.9 mm^2 region. In this study, semi-perfluoroalkyl resorcinarene (denoted as R_F-Calix-tBoc), a highly fluorinated chemical, was used as photoresist and 3-ethoxy-1,1,1,2,3,4,4,5,5,6,6,6,-dodecafluoro-2trifluoromethylhexane (denoted as HFE-7200) was used as developer. The chemical structures of all the chemicals used in this study (PI, PCBM, R_F-Calix-tBoc, and HFE-7200) are shown in Fig. 2.1(d). To verify the harmlessness of HFE-7200 to organic memory layers, the orthogonal property between PI:PCBM solution (N-methyl-2-pyrrolidone (NMP) as solvent) and organic solvent (acetone versus HFE-7200) was tested. The left picture in Fig.

2.1(e) shows that the PI:PCBM solution was completely dissolved in acetone, indicating that acetone will damage or dissolve the underlying PI:PCBM layer when used in photolithography. In contrast, the middle picture in Fig. 2.1(e) demonstrates that a good phase-separation was observed with PI:PCBM (upper layer) solution and HFE-7200 (lower layer). Furthermore, the right picture in Fig. 2.1(e) shows the insolubility of PCBM powder in HFE-7200. These results suggest that treatment with HFE-7200 will not damage the PI:PCBM layer when used in the orthogonal photolithography process.

2.2.2. Device Performance

Figure 2.4(a) represents a current-voltage (I-V) graph of a memory cell in our devices. Here, the external voltage was applied to the Au top electrode while the Al bottom electrode was grounded. This particular memory cell (Fig. 2.4(a)) was turned on at 4.1 V (or at -3.7 V) and turned off at 10.6 V (or at -8.8 V) in the positive (or negative) voltage sweep, exhibiting typical nonvolatile and unipolar switching behavior. The ON/OFF ratio of the current level of LRS to that of HRS was calculated from the data in Fig. 2.4(a) and is displayed in Fig. 2.4(b). Our microscale memory devices exhibited a high ON/OFF ratio ($> 10^6$) within a ±4 V range. The I-V characteristics of our photolithographically fabricated organic memory devices (with a cell size of 10×10 μm^2) and the other organic memory devices made by the shadow mask method (with a cell size of 50×50 μm^2) were compared, as shown in Fig. 2.4(c). Both the memory devices showed similar memory switching behavior, such as abrupt current increase at the threshold voltages (V_{th}) at which the memory cells were switched on. The current level

difference between these two types of memory devices can be explained by the cell size difference. I also observed potential multiple resistance states of our memory devices [61,68,69]. In Fig. 2.4(d), the first voltage sweep (double sweep between 0 and 7 V) switched the memory cell from the OFF to the ON state. The second voltage sweep (from 0 to 10 V) switched the cell into an intermediate state, as shown in the third sweep (double sweep between 0 and 7 V). The fourth sweep (from 0 to 15 V) switched the memory cell back to the OFF state. Results in Fig. 2.4 suggest that the memory devices fabricated by orthogonal photolithography properly operate without any intervention by fluorinated chemicals.

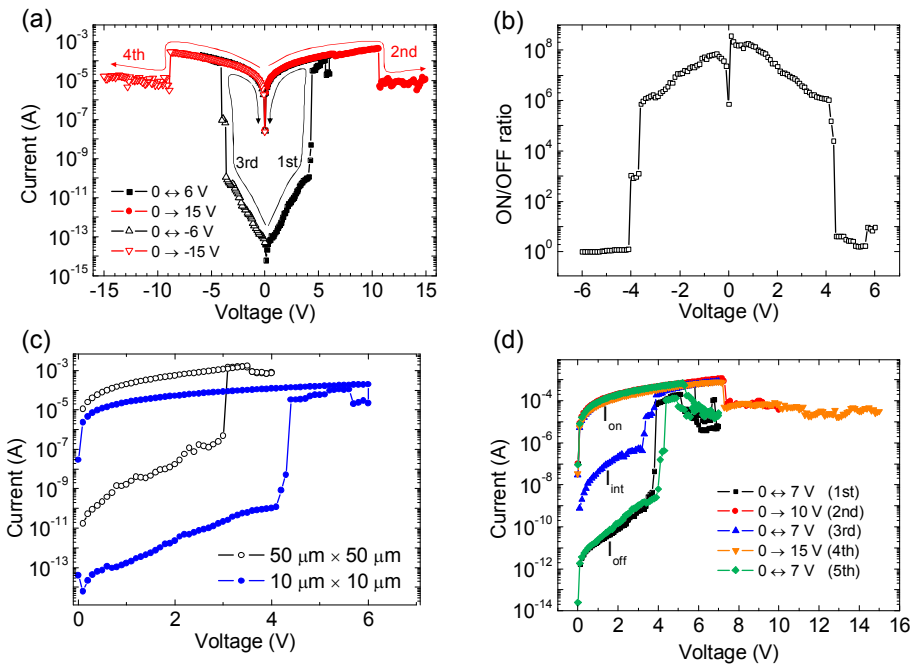


Figure 2.4 (a) I-V characteristics of an organic memory device. (b) Current ON/OFF ratio for the memory cell as a function of the applied voltage. (c) Comparison of I-V curves for 50 × 50 μm^2–sized and 10 × 10 μm^2–sized memory cells. (d) Multi-level resistance states of the organic memory devices.

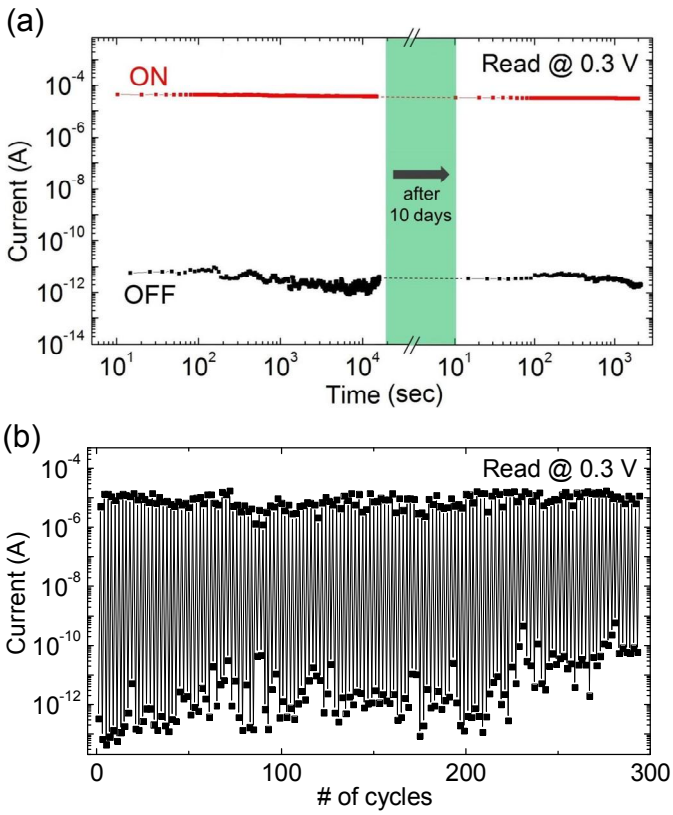


Figure 2.5 (a) Retention time and (b) DC sweep endurance test results for the 4K-bit organic memory devices. Retention time was retested 10 days after the first retention time test was performed.

To investigate the memory storage durability, a retention test was performed on our memory devices (Fig. 2.5(a)). First, the current levels of LRS and HRS were measured for 2×10^4 s with a measurement interval, Δt, of 10 s and a read voltage of 0.3 V. After 10 days of storage in a glove box filled with N_2 gas, the same device was again subjected to retention measurement, this time for 2×10^3 s. In this second retention test, the ON/OFF current ratios held at ~10^7 in magnitudes and did not exhibit any serious electrical degradation even 10 days after the first retention test. Fig. 2.5(b) shows the DC sweep endurance test used to investigate the switching performance of our organic memory devices. DC voltage sweeps were

applied to the memory device, turning it on and off repeatedly and sequentially. Although some variations of OFF-current level were observed, the memory device maintained a high ON/OFF ratio of over 10^4 during 300 repeated switching cycles. The increase of OFF current might be due to the accumulation of charge by continuous set/reset process. This limit could be improved by tuning of V_{set}/V_{reset} ratio.

2.2.3. Device Yield

Figure 2.6(a) includes a table summarizing the yield of our memory devices as well as a schematic showing the regions of the memory cells that were sampled for measurement. In the schematic, each blue square indicates a randomly chosen region of 3 × 3 memory cells that were measured, and the green rectangular region indicates 2 × 32 cells (8 bytes) that were measured. The locations of the blue square regions of the memory cells were intended to be evenly distributed on the 4K-bit organic memory devices to investigate the uniformity of the device. A number of other individually measured cells are not indicated in the schematic in Fig. 2.6(a). Among 4,096 cells, a total of 245 cells were measured, and I found 195 cells were operating properly, corresponding to a device yield of ~80%. The device failures (50 inoperative cells) are related to electrode or dielectric breakdown and to deviation in the thickness of the organic layer.

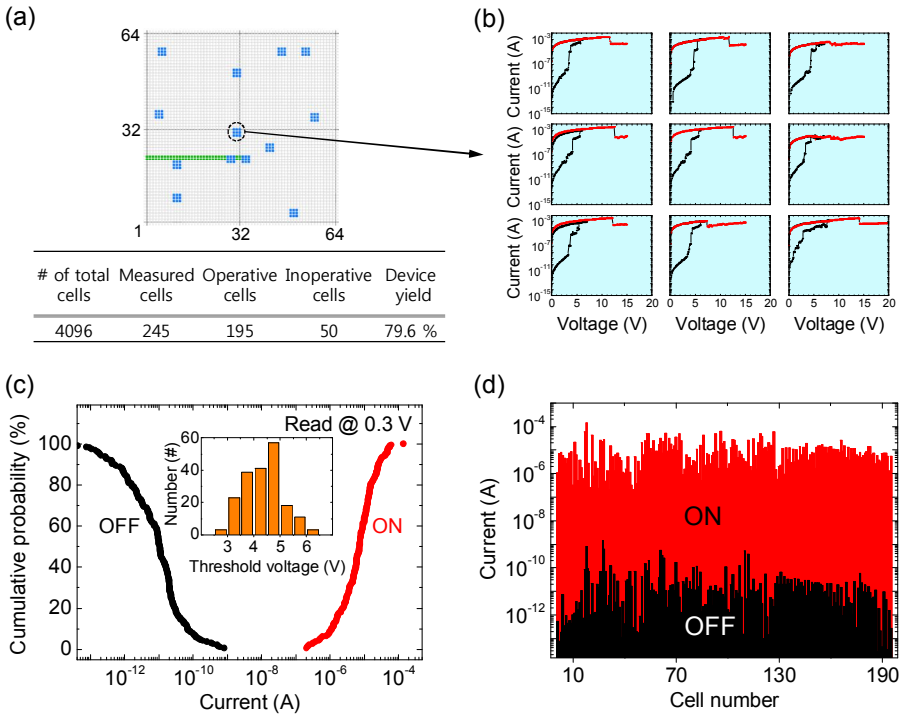


Figure 2.6 (a) A schematic of the regions selected for measurement from the 4K-bit organic memory array and a table summarizing the device yield. (b) I-V curves measured from a selected region shown in (a). (c) Cumulative probability of ON and OFF currents for all operative memory cells (195 memory cells) and the threshold voltage distribution (inset). (d) Logarithmic representation of the ON and OFF currents of all operative memory cells.

In Fig. 2.6(b), all I-V characteristics of the memory cells from a blue-square region are shown. The I-V graphs are similar to each other in terms of the current level, V_{th}, and set/reset behaviors. Measuring each I-V characteristic on selected cell, I switched off measured cell to prevent cross-talk caused by nearby cells. To check the overall device operational uniformity, the current levels of the ON and OFF states were statistically analyzed for the 195 operative memory cells within the 4K-bit array (Fig. 2.6(c)). Our 4K-bit memory devices showed a well-defined margin between the current levels of LRS and those of HRS (over 10^2 in

magnitude). Moreover, the 4K-bit memory devices showed a good distribution of threshold voltages, with values between 2.9 and 6.5 V, as shown in the inset of Fig. 2.6(c). Fig. 2.6(d) displays the statistical distribution of ON/OFF current levels in a logarithmic scale for the 195 operative memory cells. The majority of the memory cells exhibited a large difference in order (~10^{6}) between the current levels of LRS (~10^{-6} A) and HRS (~10^{-12} A).

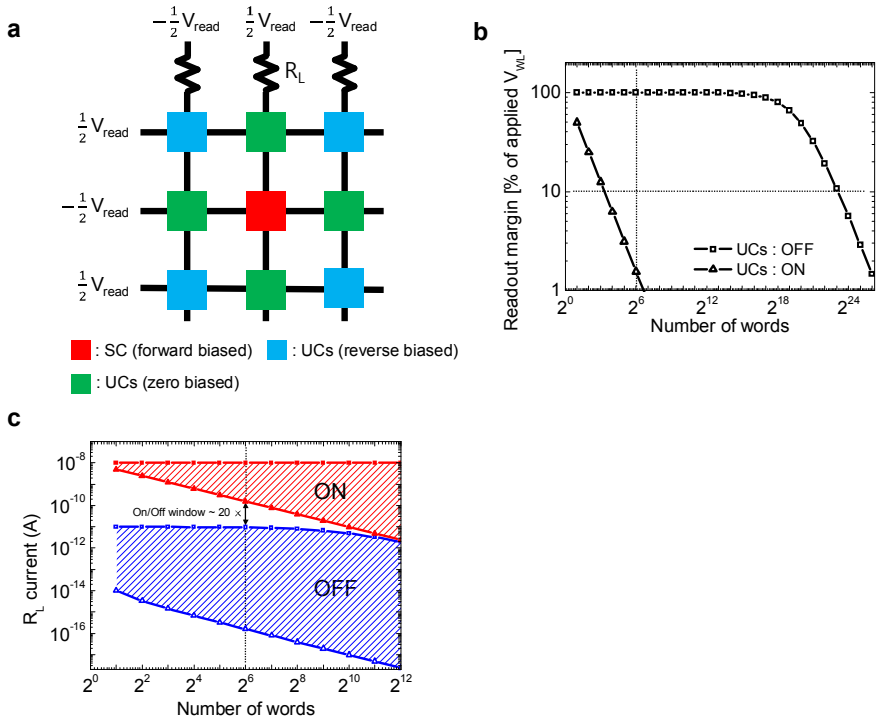


Figure 2.7 Readout margin calculation. (a) Conceptual schematic diagram of data reading operation of crossbar memory array. (b) Readout margin calculation data based on the schematic Fig. S9 (a). The square symbol indicates the readout margin for best case and the triangular symbol indicates the worst case. (c) Graph of calculated currents through load resistor (R_L) with the 4 cases of SC being on or off and in the best case or the worst case. On state currents of selected cell with arbitrary arrangement of UCs' states are indicated by red dashed region, while Off state currents of selected cell with same situation are indicated by blue dashed region.

2.2.3. Readout margin calculation

Our device have no selector element, which causes the cross-talk problem. The cross-talk interference problem between memory cells can occur due to leakage current paths through neighboring cells with low resistances in cross-bar architecture array structures. However, our memory device lacks the selection elements yet. In this chapter, I chose one of the measurement schemes (i.e., +1/2 V_{read} or -1/2 V_{read} measurement scheme) and I studied how this measurement scheme can be applied to our memory array devices. Often, many researchers studying inorganic memory array devices make a model of the read operation scheme and calculate the readout margin (RM) for their cross-bar type memory arrays. Specifically, they model the circuit in which they biased all the bit lines and the word lines and calculate the readout margin based on the parameters measured from I-V characteristics of a single memory cell. This calculation process is very useful for studying memory performances of integrated cross-bar type memory array.

Figure 2.7(a) shows a measurement scheme describing the data reading operation of our 4K-bit integrated organic memory array devices. In this scheme, a load resistor (RL) is attached to the each column line (bit line) as a simple and common method for determining the state of a memory cell by constructing a voltage divider. Here, a selected cell (SC) for specific sensing is forward biased with V_{read} (0.3 V in our study) and unselected cells (UCs) on selected bit or column line are zero biased, and remaining UCs are backward biased with -Vread.

However, the exact voltage across each cell is neither $\pm V_{read}$ nor 0 V due to RL. And I converted the cross-bar array to a simple equivalent circuit template to calculate RM [70,71]. RM indicates the maximum difference between the voltages across the RL in the case of SC being ON or OFF. A larger RM value guarantees the discrimination of ON/OFF state of SC. For simple calculation of RM in an ideal situation, I assumed negligible interconnect resistance and the same current level of all memory cells. In the real situation, RM would be affected by the interconnect resistance and individual variation of current level of each cell. Parameters for calculation are determined from the read current statistics (Fig. 2.6(c)). The representative values for ON and OFF resistance (R_{ON} and R_{OFF}) are derived from the median values of the read current statistics; the representative R_{ON} is 3×10^4 Ω and the representative R_{OFF} is 3×10^{10} Ω, and optimized RL is 3×10^7 Ω). For the calculation of RM, I compared the two cases of UCs' states, one case is that all the UCs' states are OFF (which is the best case) and the other case is that all the UCs' states are ON (which is the worst case). The RM values were calculated as a function of the number of word lines, as shown in Fig. 2.7(b). In the best case, the sneak current through UCs is minimized, therefore the RM calculation shows the highest RM. Because our memory devices have high ON/OFF ratio (~106), the 223 = 8,388,608 word lines (with the same number of bit lines) integration of organic memory would present ideally over the 10% of RM in the best case. For our integration of 28 = 64 word lines, RM reaches 99.8% in the best case. However, in the worst case, the RM value rapidly decreases with increasing integration. RM can reach only 1.6% with 64 word lines integration in the worst case.

I also calculated the sensing current through RL as a function of the number of word lines, as the result is shown in Fig. 2.7(c). The square symbols indicate the sensing currents while SC is ON (red) or OFF (blue) state in the best case. And, the triangular symbols indicate the sensing currents in the worst case. In cases between the best and worst case (i.e., when each UC has arbitrary state), the sensing current of SC is positioned in the hatched region. Although RM value is not good for the worst case, still I can discriminate the state of SC by at least 20 fold difference between ON/OFF currents with arbitrary UCs' states in 64 word line-integration of our memory devices. However, the read operation scheme has an energy dissipation due to reverse biasing at UCs, and also the estimated RM values in the worst case may not be suitable for the real device application. These problems can be avoided effectively when we use memory arrays having selection elements such as one diode-one resistor (1D-1R) architecture. In 1D-1R structure, the resistance of reverse biased cell in ON state is comparable to the R_{OFF}, therefore the resulting RM value in the worst case is expected to be greatly improved.

2.3. Further application to flexible organic memory

Recently, fabrication of organic memory devices on the flexible substrate such as polyethylene naphthalate (PEN) or poly(ethylene terephthalate)(PET) have been studied [57,62,63,72–74]. However, the integration of the flexible organic memory devices has not been beyond 64 bits and the individual cell size of cross-bar structured organic memory devices has usually been limited to several hundreds of microns (μm) using shadow mask method [57,62,63,72–74]. The solution is to use fluorinated photoresist (such as semiperfluoroalkyl

resorcinarene) and solvents (such as hydrofluoroethers) as I mentioned above which are miscible to each other and orthogonal to most organic materials and flexible substrates.

In this study, I demonstrate the integration of flexible and microscale organic nonvolatile resistive memory devices with 4,096 bit (64 × 64) organic memory cells in 1.9 × 1.9 mm^2 with cross-point architecture on a plastic substrate. The fabrication of the device was possible by using orthogonal photolithography process using fluorinated resist and solvents. And I studied the electrical characteristics of our flexible organic memory devices under different bending conditions (bending radius of 10 mm and 5 mm).

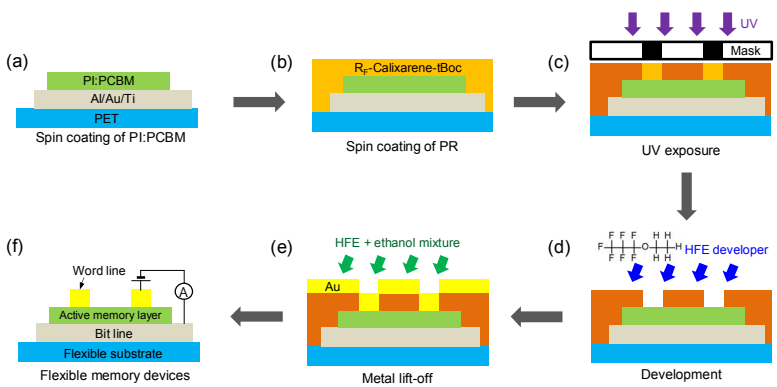


Figure 2.8 The schematics of fabrication process and optical image of the flexible and microscale organic memory devices.

Figure 2.8 shows the schematics of fabrication process and optical image of the flexible and microscale organic memory devices on a plastic substrate. The fabrication process is almost same with that on hard substrate, the difference comes from the bottom electrode formation. First, a PET substrate was prepared and ultrasonically cleaned using acetone, isopropanol, and de-ionized water. Then, Al (20 nm)/Au (15 nm)/Ti (5 nm) were deposited for

bottom electrodes on the PET substrate. Here, Au/Ti bilayer (Ti as an adhesion layer and Au as a buffer layer) reduces the oxidation of the bottom Al electrode caused by the PET substrate material [62]. The bottom electrodes with a width of 10 μm were patterned by the standard photolithography and lift-off process. Then, the prepared memory solution (PI:PCBM) was spin coated onto the substrate at 1500 rpm for 35 s, followed by soft-baking on a hot plate at 120 °C for 5 min. The PI:PCBM layer on the substrate was hard-baked on a hot plate at 200 °C for 2 hours (see Fig. 2.8(a)). Then the prepared fluorinated photoresist solution was spin coated at 1500 rpm for 50 s, followed by baking process at 75 °C for 3 min under yellow light (Fig. 2.8(b)). Subsequently, the coated photoresist film was exposed under UV light through a photomask. After post-exposure baking at 75 °C for 3 min, the photoresist film was developed by HFE-7200 and dried with N_2 gas (Fig. 2.8(d)). Then 30 nm-thick Au layer was deposited on the developed samples as top electrodes. Finally, for the flexible and microscale organic memory array devices, the sample was lifted off in an ethanol (5 vol%)-HFE-7200 (95 vol%) mixture to leave patterned (Fig. 2.8(e)). The flexible condition was accomplished by attaching samples on surface of the semicylindrical plastic mold.

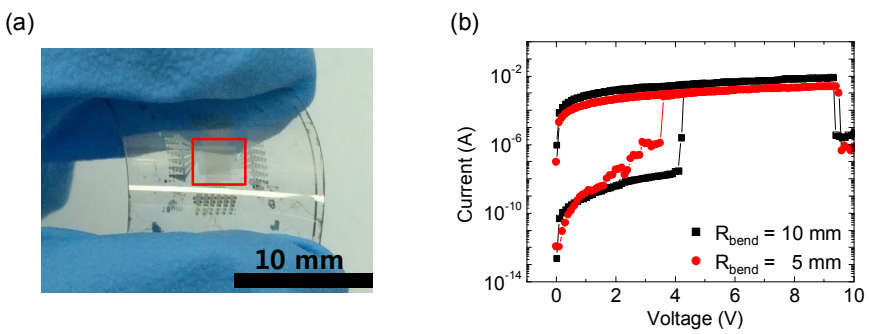


Figure 2.9 (a) Optical image of fabricated flexible microscale organic memory devices.

(b) I-V characteristics of a flexible and microscale organic memory cell measured in bending conditions with a bending radius of 10 mm and 5 mm.

The optical image of the finished 4K-bit integrated and microscale organic memory devices on a PET substrate is shown in Fig. 2.9(a). In a 1.9×1.9 mm^2 region, 4,096 of micro-sized organic memory cells are integrated with crossbar structure. Figure 2.9(b) shows the representative current-voltage (I-V) curves of the flexible microscale organic memory devices of PI:PCBM that were acquired under bending configurations with a bending radius (R_{bend}) of 10 mm and 5 mm. The external voltage was applied to the Au top electrode while the Al bottom electrode was grounded. The ON state (that is the low resistance state) and OFF state (that is the high resistance state) were made in the same voltage polarity, which is called "unipolar-type" resistive switching behavior. It has been reported that PI:PCBM composite organic memory devices exhibit rewritable unipolar memory switching [62–64,75,76]. The particular memory cell was turned on at ~4.1 V and 3.7 V and turned off at ~9.5 V and 9.3 V in the 10 mm and 5 mm bending conditions, respectively. In both bending conditions, the flexible microscale organic memory device showed similar ON/OFF switching and stable current behaviors in the reading voltage region (< 0.5 V) with a high ON/OFF ratio (I_{ON}/I_{OFF} ~10^5). The switching mechanism of PI:PCBM composite can be explained by a charge-trapping mechanism, as nano-sized PCBM clusters embedded in PI matrix take the role of charge trapping center [77].

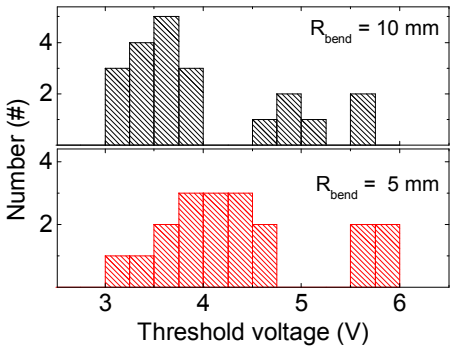


Figure 2.10 Distribution of the threshold voltage values for the bending radius of 10 mm (upper graph) and 5 mm (lower graph).

Figure 2.10 shows the distribution of threshold voltages from 20 randomly chosen memory cells in both 10 mm and 5 mm bending conditions. In these bending conditions, the threshold voltages were distributed in the range between 3 and 6 V and the mean values of threshold voltages were found to be ~4.0 V and 4.5 V for 10 mm and 5 mm bending conditions, respectively. The similar threshold voltage distributions among the bending conditions indicate that the individual memory devices can be switched ON uniformly without degradation due to bending conditions [63].

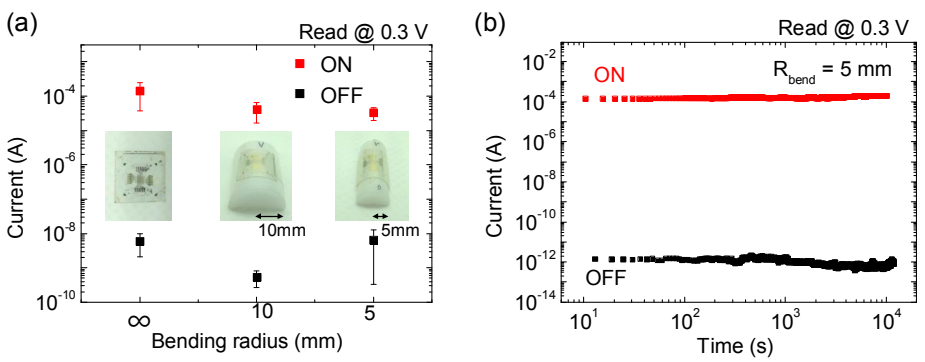


Figure 2.11 (a) Read current measured at 0.3 V for the ON and OFF states in different bending conditions with a bending radius of ∞ (flat), 10 mm, and 5 mm. (b) Retention time test results for the flexible and microscale organic memory device.

Figure 2.11(a) shows the ON/OFF current values measured at read voltage of 0.3 V from about 20 memory cells for three bending conditions (R_{bend} = ∞ (flat), 10 mm, and 5 mm). The bending configurations are displayed in the inset of Fig. 2.11(a). I found that the ON/OFF ratio of our flexible microscale organic memory devices maintained about 10^4 and it did not undergo significant electrical degradation under the different bending conditions. I also investigated the memory storage durability. The memory retention test was performed on our flexible memory devices and the results are shown in Fig. 2.11(b). Our flexible and microscale organic memory device exhibited a long retention time up to 10^4 seconds under the bending condition (R_{bend} = 5 mm) maintaining very high ON/OFF ratio (~10^7) at 0.3 V bias.

All these results suggest that our devices presented good nonvolatile resistive memory behaviors under the various bending configurations. The proper operating microscale organic memory devices indicate that the orthogonal photolithography method did not make any serious damage to active memory layer, flexible substrate, and electrodes. And the high integration of microscale memory devices was possible due to large-area processability of photolithographic method, while other studies using shadow mask couldn't demonstrate microscale devices. The similarity of electrical characteristics have been also observed in various flexible organic memory devices in macro scale [57,62,63,72–74]. The similarity for different bending conditions is due to thin active memory layer. The thickness of spin coated PI:PCBM layer is known to about 20 nm. Then the bending strain induced by the length differences between top and bottom layer of PI:PCBM layer would be (*Film thickness*

$/R_{bend}$) = $4 \cdot 10^{-6}$ for 5mm bending radius, which is very small so that interval between nanoscale PCBM clusters are almost not changed with bending conditions. Therefore with ignorable deformation, the active film can function uniformly under mild bending conditions.

2.4. Conclusions

In summary, I fabricated 4K-bit highly integrated and microscale resistive nonvolatile organic memory devices with a 10×10 μm^2 cell size in a 64×64 cross-bar array structure. The fabrication of 4K-bit and microscale devices was made possible by the usage of fluorinated organic materials and solvents in the orthogonal photolithography process. Our 4K-bit organic memory devices also exhibited good device operation performance in terms of uniformity, retention, and endurance characteristics. Furthermore, I demonstrated the integration of flexible and microscale organic resistive memory devices on a plastic substrate. This study may foster microscale organic electronics applications for high-capacity information storage.

Chapter 3. Noise analysis on organic resistive memory

3.1. Introduction

Organic material-based electronic devices have recently taken significant attention for their various advantages, including low manufacturing cost, large area processing capabilities, flexibility, and printing processes [48,78,79]. Especially, organic resistive memory devices, in which active polymer materials possess at least two stable resistance states, have been extensively studied for their promising potential for use in storage media [1,53,55]. Many studies on organic memory have focused on scientific and technical issues of the materials, device structures, switching mechanisms, and performance enhancement [1,55,77,80,81]. However, because of the strongly disordered polymer structures, a consensus on the mechanisms of organic resistive memory has not been achieved.

In particular, the charge conduction in organic memory materials is greatly influenced by the traps that are present in the bulk of the organic memory material or at the interface near the electrodes. In addition, bistable switching can occur from the accumulation of trapped charges, which affect the injection of charges into the organic material and often produce a negative differential resistance (NDR) region in the current-voltage characteristics [69,77,82]. The NDR has been frequently observed in unipolar-type resistive memory from various nanocomposite systems, in which inorganic or organic nano-sized particles are embedded in an insulating matrix [69,77,83,84]. Some groups explained the NDR phenomenon as

the formation and rupture of conducting filaments in organic or inorganic oxide materials under an applied bias [85,86]. Other groups explained the NDR phenomenon as trapping or detrapping of charges at trap [77,84]. However, the switching mechanism for the organic nanocomposite system is still under debate, and few studies have focused on and elaborated the NDR and its derivative intermediate resistive states.

The existing low-frequency noise (LFN) studies provided deep insights into the inherent charge transport mechanisms of various disordered systems, *e.g.*, organic semiconductor [87], metal-molecule-metal junction [88,89], inorganic filamentary memory [85], and granular systems [90]. With an external electric field, the noise data could provide information regarding charge trapping-detrapping phenomena and the percolating behavior of the conduction pathways through the media with randomly distributed trap sites. In this study, I investigated the LFN characteristics of a composite of polyimide (PI) and phenyl-C61-butyric acid methyl ester (PCBM), focusing on the NDR and the multi-level resistive states. The current noise was investigated in both time and frequency domains. I observed that the current noise power spectral density exhibited $1/f^{\gamma}$ noise characteristics, where γ is ~ 1 at low bias and ~ 1.5 for high bias in the NDR region. In addition, the *1/f* noise at low bias increased with a power-law scaling as the resistance of the nanocomposite increased, indicating a percolating behavior. We related the conductive phase fraction represented by the ratio of the charge-occupied trap density to the total trap density with the applied bias regarding the charge trapping-detrapping in the NDR region. The percolating behavior and NDR in the

nanocomposite memory devices were explained as the modulation of the conductive phase fraction with applied field in the NDR.

3.1.1. Conduction and switching mechanism of organic resistive memory

Organic nanocomposite memory devices have typically shown non-ohmic behavior at their operation voltage from 0.1 V to 3 V, which does not allow the formation of metallic conductive filaments [91]. In this regard, many research groups have concluded that various traps have a critical role in the formation of conducting paths in the organic active layers by comparing current-voltage characteristics with well-established charge transport mechanisms, such as Poole-Frenkel conduction, space charge limited current, and Fowler-Nordheim tunneling [1,92–94]. In particular, Bozano et al. have investigated the origin of NDR in organic nanocomposite memory devices where aluminum granules are embedded in an organic matrix (Alq_3) [77]. As their organic memory devices showed similar electrical behaviors compared with those of inorganic metal-insulator-metal diodes where gold atoms are dispersed in a silicon oxide insulating layer by the electroforming process, Bozano et al. concluded that the transport and switching of organic nanocomposite memory devices are based on Coulomb blockade. According to their statements, charge carriers are trapped on metallic granules at the NDR regime forming space-charged field, so that Coulomb blockade occurs and resistance decreases (off-state). However, the off-state is usually observed in a pristine device, which is inconsistent with the previous statement [55]. Moreover, in a recently reported study for the impedance

characterizations of organic nanocomposite memory devices, the Coulomb blockade-based mechanism was discluded to explain the state-independent capacitive contribution in the AC-spectra, and it was suggested that the mechanism is based on the formation of localized current pathways inside the organic material [95]. However, the causal relation between NDR and its derivative IRSs are still not clearly understood.

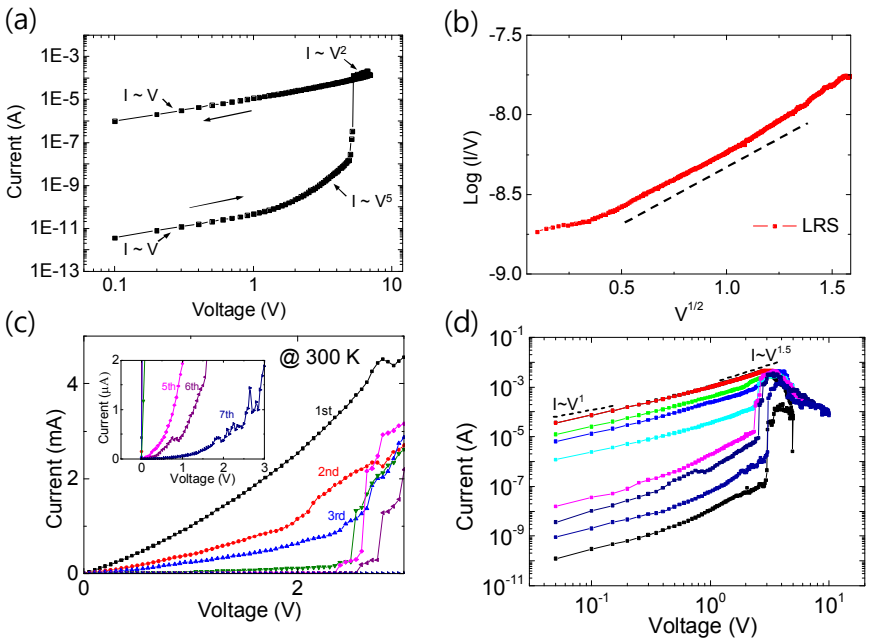


Figure 3.1 (a) I-V characteristics exhibiting space-charge-limited-current behavior in PI:PCBM memory. (b) I-V characteristics of LRS of PI:PCBM memory fitted with Poole-Frenkel conduction (c) linear-scale I-V and (d) log-log scale I-V characteristics of IRSs of PS:PCBM memory.

The conduction behavior of LRS in PI:PCBM memory was not ohmic as shown in nonlinear relationship from I-V characteristics. From fitting the I-V curve to various conduction mechanisms, such as thermionic emission [96], Fowler-Nordheim tunneling [97], space charge limited cuonduction (SCLC) and Poole-Frenkel conduction [98], I found that SCLC and Poole-Frenkel conduction

mechanism showed the best fit to the measured I-V curve; $I \propto V$ at low voltage bias (< 0.5 V), $I \propto V^5$ near switching voltage (trap-limited regime), and $I \propto V^2$ at on state with high bias (trap-filled limit) for SCLC (Figure 3.1(a)); $V^{1/2}$ Log(I/V) $\propto V^{1/2}$ for Poole-Frenkel conduction mechanism (Figure 3.1(b)). At on state, distinguishing Poole-Frenkel conduction and SCLC is difficult because both fitting equation exhibits ohmic conduction at low bias and $I \propto V^2$ at high bias.

Furthermore, the I-V characteristics of the intermediate resistive states (IRSs) of PS:PCBM nanocomposite memory devices are shown in Fig. 3.1(c). In linear scale graph, all the IRSs showed non-ohmic behavior in 0.2–3 V, i. e., the main conduction mechanism of PS:PCBM memory would not be a conductive filamentary conduction regardless of the resistive states. In the log-log scale plot (Fig. 3.1(d)), the I-V relation around 0.1 V was ohmic ($I \propto V$). Increasing the voltage bias, I-V relations become non-ohmic ($I \propto V^{\beta}$, $\beta > 1$). At the voltage close to the switching voltage, β values were in the range between $1.3 < \beta < 3$.

From the I-V curve shape, at least I can conclude that the metal filament formation is less related with the conduction in our resistive memory devices. Because Both SCLC and Poole-Frenkel states the electric conduction with trap contribution, the switching mechanism and the electric transport in the organic nanocomposite memory devices can highly attributed to the trap-mediated conduction.

3.1.2. Noise in disordered system

Strongly disordered and inhomogeneous samples can have hooge parameter many orders higher than 2×10^{-3}, as the effective number of free charge carriers

may be much smaller than N_c. In a real disordered entity, the noise value variation comes from the constriction and the bottleneck effect of the electric current flow. Then the parameters related with disorder in the system can determine the noise variation. The parameters can be the ratio of conducting phase to the insulating phase, distribution of defects or traps and the dimension of the system. These consideration leads to the percolation theory. To understand noise behavior in disordered system, a simplest model, the random resistor network is usually considered [4].

In a random resistor network, the relative power spectral density and resistance exhibits a scaling behavior in the condition where the conductive phase fraction φ is higher than a critical conductive phase fraction φ_c, described as [4]

$$S_I(f)/I^2 = S_R(f)/R^2 = \frac{\sum \tilde{s}(f)_m r_m^2 i_m^4}{\left(\sum r_m i_m^2\right)^2} \propto (\varphi - \varphi_c)^{-\kappa} \text{ at } \varphi > \varphi_c \tag{3.1}$$

$$R \propto (\varphi - \varphi_c)^{-t} \text{ at } \varphi > \varphi_c \tag{3.2}$$

where r_m denotes the m-th primitive resistor in the percolation network, i_m is the fractional current flowing through r_m, $\tilde{s}(f)_m$ is the spectral density of fractional noise of r_m, and R is the total resistance of the percolating network. Note that in the above relations, the resistance R and relative power spectral density S_I/I^2 diverge as φ approaches φ_c from the conductive side. If the percolating network has smaller current pathways with lower φ (when approaching φ_c), a large amount of current becomes concentrated on a few current pathways. Therefore, the higher relative noise from the network can be induced. Because it is difficult to obtain the

exact value of φ from experiments, the scaling behaviors of S_I/I^2 and R can be combined to the experimentally obtainable scaling relation as

$$S_I(f)/I^2 \propto R^{\omega} \text{ at } \varphi > \varphi_c \tag{3.3}$$

where the exponent ω denotes κ/t.

3.2. Experimental setup and measurement

For the active nanocomposite organic memory material (PI:PCBM), 2 ml of 3,4,3',4'-biphenyltetracarboxylic dianhydride-p-phenylene diamine (BPDA-PPD) solution (10 wt% in N-Methyl-2-pyrrolidone(NMP)) as PI precursor and 0.5 ml of PCBM solution (0.5 wt% in NMP) were mixed and then diluted with 11.3 ml of NMP to control the active layer thickness. First, a SiO_2 (270 nm thick)/Si substrate was prepared and cleaned using acetone, isopropanol, and de-ionized water for 10 min at each step. The 30-nm-thick Al bottom electrode lines with 100 μm line width were fabricated using a shadow mask patterning. To enhance the film uniformity, the Al bottom electrodes were exposed to UV-ozone for 10 min [57]. The prepared memory solution was spin coated onto the substrate, followed by soft-baking on a hot plate at 120 °C for 5 min and then hard-baking on the hot plate at 300 °C for 30 min in a N_2-filled glove box. Then top electrodes of a 30 nm-thick Au layer were deposited on the active memory layer. The PI:PCBM layer thickness was about 20 nm.

The I-V characteristics of the devices were measured with a semiconductor parameter analyzer (Keithley 4200 SCS) and a probe station system (JANIS Model

ST-500) [89]. Figure 3.2 shows the noise measurement setup in our experiments. For noise measurement, I used a spectrum analyzer (Stanford Research SR780) and ground-isolated 16-bit analog-digital converter (ADC) to measure low-frequency noise (LFN) on frequency and time domain, respectively. A battery-powered low-noise current amplifier (Ithaco 1211) was used for LFN measurements. A 16-bit digital-analog converter (DAC) was used to apply bias. A digital multimeter (Agilent 34401A) was used to get average electric current coinciding with the noise power spectral density measurement. All the measurements were performed in vacuum environment and room temperature.

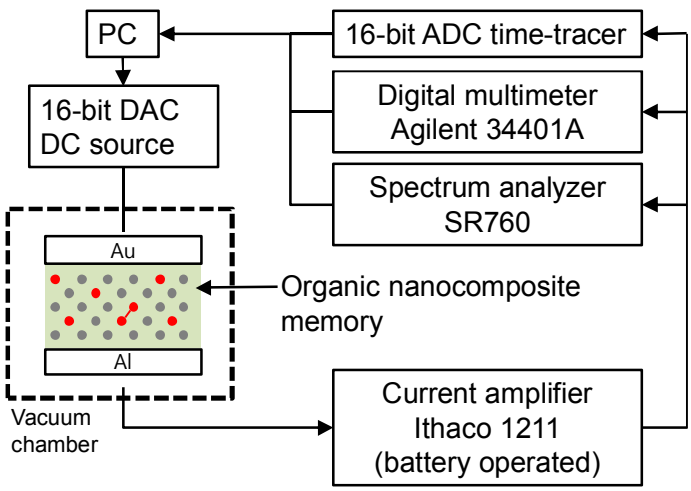


Figure 3.2 Schematic of the noise measurement setup.

3.3. 1/f noise spectra

A nanocomposite organic material of PI:PCBM (Figure 3.3(a)) was used as an active material in the resistive memory device structure. In PI:PCBM nanocomposites, PCBM clusters as electron acceptors are wrapped by a PI insulating matrix. PI:PCBM has been demonstrated to be a promising candidate for the organic nonvolatile resistive memory material due to its stable electrical

bistability [60–62]. With a two-terminal device configuration, a PI:PCBM nanocomposite was found to exhibit unipolar switching behavior with a change of resistance, in which the same voltage polarity is used to write and erase the memory states [60–62].

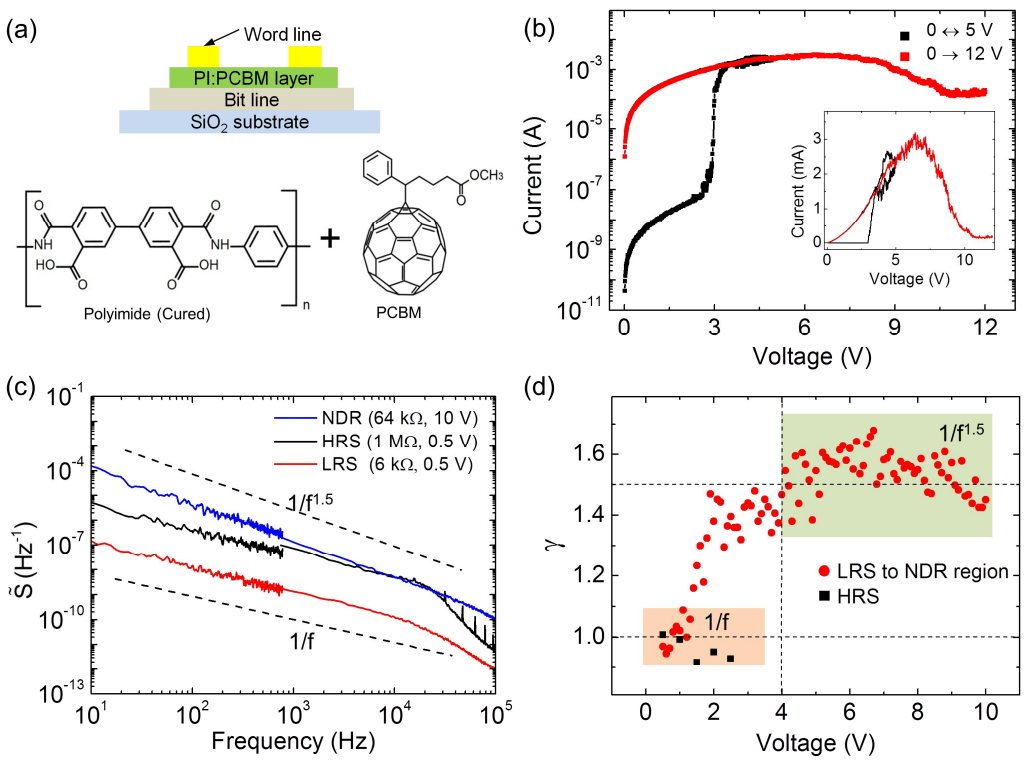


Figure 3.3 (a) Molecular structures of PI and PCBM. (b) Bistable I-V characteristics of a PI:PCBM device plotted on a semilogarithmic scale and on a linear scale (inset). (c) Relative power spectrum current noise of LRS, HRS, and NDR. (d) The value of the γ as a function of applied voltage bias in the LRS, HRS, and NDR.

Figure 3.3(b) displays the typical current-voltage (I-V) characteristics of a PI:PCBM memory device on a semilogarithmic current scale. The inset plot in Fig. 3.3(b) shows the same I-V data on a linear current scale. Initially, the PI:PCBM is in a high-resistance state (HRS, > 1 MΩ). When the applied bias is swept from 0 to 5 V, the PI:PCBM underwent resistive switching, in which the HRS became the

low-resistance state (LRS, < 10 kΩ). When I swept the bias back to 0 V, the LRS was maintained, exhibiting a high current level. While sweeping the bias from 0 to 12 V, the NDR was observed from approximately 4 V with unstable and noisy current behavior. When applying a bias over 10 V, the PI:PCBM switched back to the HRS. It is widely accepted that, in the case of nanocomposite organic nonvolatile resistive memory devices, trapping-detrapping of charge carriers occurs at the nano-clusters embedded in the organic insulating matrix [80,99,100].

Figure 3.3(c) shows the relative current noise power spectral density ($\tilde{S} = S_I / I^2$) of the LRS, HRS, and NDR measured for a PI:PCBM memory device. The noise characteristics of the HRS and the LRS were measured at a read voltage of 0.5 V, and those for the NDR were measured at 10 V. Clear *1/f* noise characteristics were observed in both the HRS and LRS in the frequency range between 10 and 10^4 Hz, with the noise level of the HRS being 2-3 orders of magnitude higher than that of the LRS. The roll-off behavior at f > 10^4 Hz is attributed to inevitable capacitive coupling [101]. Unlike the LRS and the HRS, in the NDR region, $1/f^{1.5}$ noise characteristics were observed. This result suggests that the main noise source in the NDR region is different from that of the HRS or LRS. Figure 3.3(d) summarizes the exponent γ of the $1/f^{\gamma}$ signal characteristics for the LRS, HRS, and NDR cases, measured from 0.5 to 10 V. In the HRS, the memory device exhibited *1/f* noise consistently by showing an exponent of $0.9 < \gamma < 1$ until the device was switched to the LRS. In the LRS, the device showed *1/f* noise behavior when the applied bias was less than 1 V. When the applied bias was over 1 V, the exponent γ gradually increased, and it remained in the range of $1.4 < \gamma < 1.6$ when the bias was greater than 4 V. The increase of the exponent from the LRS

to the NDR can be attributed to the onset of trapping-detrapping of charges in deep trap levels [102,103]. I will further discuss this trapping-detrapping behavior later.

To confirm the role of PCBM molecules embedded in PI matrix for memory operation, I examined the electrical and noise characteristics of a PI thin film that did not contain PCBM molecules. Figure 3.4(a) shows an I-V curve of PI layer. The PI layer did not exhibit any reliable memory switching. In this figure, a sudden increase in current at a high bias larger than 10 V can be attributed to the dielectric breakdown of the PI layer. This phenomenon was neither repetitive nor consistent, thus cannot be considered as bistable switching memory.

The noise characteristics of PI layer are displayed in Fig. 3.4(b). PI layer exhibited *1/f* type noise for a voltage range between 0.5 and 9 V with no $1/f^{1.5}$ type noise characteristics that was observed in PI:PCBM memory samples. Therefore I can conclude that the PCBM molecules play an important role for the bistable switching behavior.

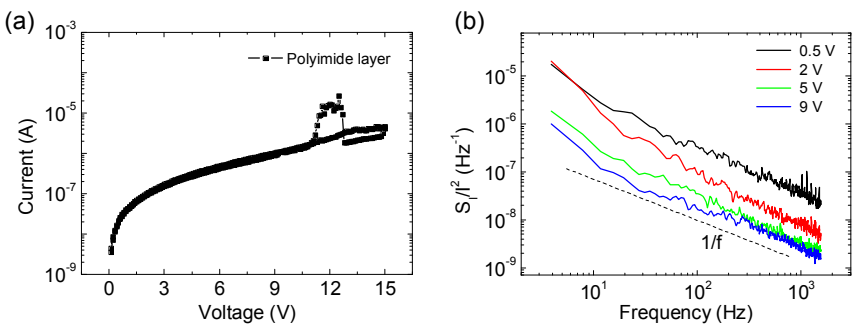


Figure 3.4 (a) I-V curve and (b) the 1/f type noises with range of voltages on the PI thin film.

3.3.1. Scaling behavior between noise and resistance

Various resistive memory devices based on oxide insulators or nanocomposites, including PI:PCBM, often exhibit intermediate-resistance states (IRSs) [61,69,85]. Usually, IRSs can be approached by setting a compliance current or modulating the voltage at which the device is switched off. The PI:PCBM has IRSs of the latter case, which means that modification of the voltage sweep end (V_{end}) in the NDR region causes the device to enter into various current states. In this regard, the HRS and the LRS can be understood as the highest and the lowest resistance states among the IRSs, respectively. In Figure 3.5(a), the representative I-V characteristics of a PI:PCBM memory device exhibiting IRSs are presented. Starting from the LRS, the applied bias sweep was repeatedly performed by changing the value of V_{end} of each sweep. The value of V_{end} is located in the middle of the NDR region, and the larger the value of V_{end}, the lower the current level becomes. Each IRS was stable, as an IRS could maintain its resistivity under the read voltage of 0.5 V during the noise measurements.

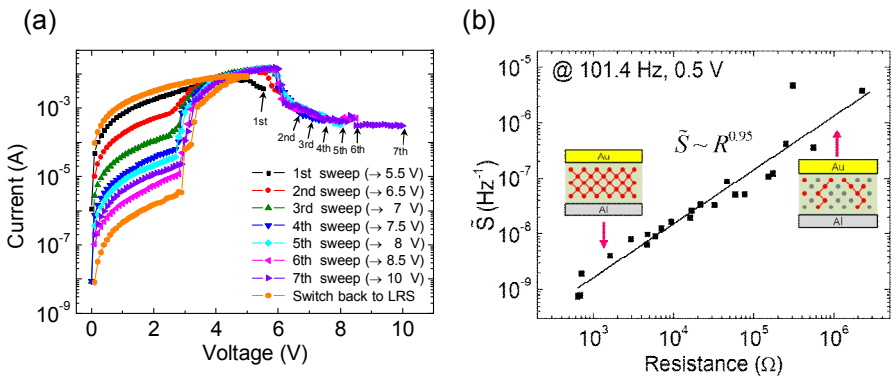


Figure 3.5 (a) I-V characteristics of PI:PCBM exhibiting IRSs. (b) Power-law relationship between the relative current noise power spectral density $\tilde{S}$ and the resistance R of the IRSs, with f = 101.4 Hz and 0.5 V.

The existence of IRSs leads us to the noise characterization of the IRSs regarding each state as a current distribution through the resistance network of a percolation system [85]. In the PI:PCBM nanocomposite system, the trap sites can be considered to be elementary bonds or sites in percolation theory. In percolation theory, it is known that the relationship between the relative current noise power spectral density $\tilde{S}$ and resistance *R* exhibits a scaling behavior in the condition when the conductive phase fraction φ (the physical meaning of this parameter is the portion of the conducting sites in the media) is larger than a critical phase fraction φ_c and this relationship can be written as [4]

$$\tilde{S} = S_I(f) / I^2 = S_R(f) / R^2 \propto R^{\omega} \quad (\text{at } \varphi > \varphi_c). \tag{3.4}$$

Here, the meaning of φ_c is that the memory system becomes from insulating to conductive state by forming a conductive percolating network at φ_c . Also it is well known that inhomogeneous current distribution in percolation system induces higher $\tilde{S}$ [4,85]. As a PI:PCBM device can reach intermediate resistive states, I could obtain $\tilde{S}$ and *R* for a number of resistance values in IRSs. In addition, these IRSs exhibit *1/f* noise at 0.5 V, as in the cases of the LRS and the HRS. In Fig. 3.5(b), the power law relationship between $\tilde{S}$ and *R* of IRSs is shown. Each resistance state is obtained by modification of the value of V_{end} in the NDR region. Because the resistance fluctuation in the NDR is large, even for the same V_{end}, slightly different resistance states could be approached. However, the tendency that higher V_{end} leads to a higher resistive state was maintained. I found that the magnitude of $\tilde{S}$ *versus* the resistance of the IRSs exhibited a power law behavior

as ω = 0.95 in eq.(3.4), which was consistently observed with the other PI:PCBM memory device studied. A similar scaling behavior has been observed in various composite systems. For example, values of ω equal to 1.16, 1, and 0.77 were reported for composite systems of PANI:PMMA [104], AgPt:tetrafluoroethylene [105], and carbon black:polymer [106], respectively, in which the scaling behavior was confirmed by varying the ratio of the conducting particles to the embedding insulating matrix. Note that a scaling behavior but with a different power exponent of ω = 1.8 has been reported for a filamentary-type switching NiO resistive memory characterized at room temperature [85].

3.4. Telegraphic noise

The current fluctuations in the time domain were measured. In Fig. 3.6(a), current traces were recorded over 0.2 s at room temperature with applied bi ases in sequence and each data point was acquired with a time interval of 2 μs. The corresponding histograms of the current traces are plotted in Fig. 3. 6(b). Figure 3.6(c) shows the schematics explaining the behaviors of the tim e-dependent current fluctuation at each bias condition. First, I biased a PI:P CBM device in the LRS with 0.5 V. The device exhibited a simple Gaussia n distribution of time-dependent current fluctuation. The distribution of curr ent values has a single peak at the average current value (top figure in Fig. 3.6(b)). However, when I biased the device in the NDR with 5 V and 9 V, the device exhibited abrupt alterations of current values. At 5 V bias in the NDR, at least five peaks were observed in the current histogram; in compari son, two distinct peaks were observed in the current histogram for the case

of 9 V bias in the NDR (middle two figures in Fig. 3.6(b)). After the 9 V bias in the NDR, I applied 0.5 V to cause the PI:PCBM to change to the HRS. The device in the HRS also exhibited a Gaussian distribution of curre nt values (bottom figure in Fig. 3.6(b)) as is the case in the LRS, but the r elative standard deviation (RSD, which is given as $\sigma/\mu \times 100$ %, where μ and σ are the average and standard deviation of current level, respectively) value for the HRS (8.88%) was larger than that (0.15%) for the LRS by ap proximately two orders of magnitude. Because RSD can represent the relativ e noise amplitude, the HRS shows more noisy behavior than LRS does. In Fig. 3.7, the time traces of (a) LRS, (b) IRS and (c) HRS are shown. With 0.5 V bias, each current trace showed single peak of Gaussian distribution of current values. Noise to signal (NTS) ratio of LRS, IRS, and HRS were 1.3, 7.6, and 40 %, respectively. The increase of NTS value with increasing R is consistent with the relation between $\tilde{S}$ versus R shown in Fig. 3.5(b) in the main manuscript.

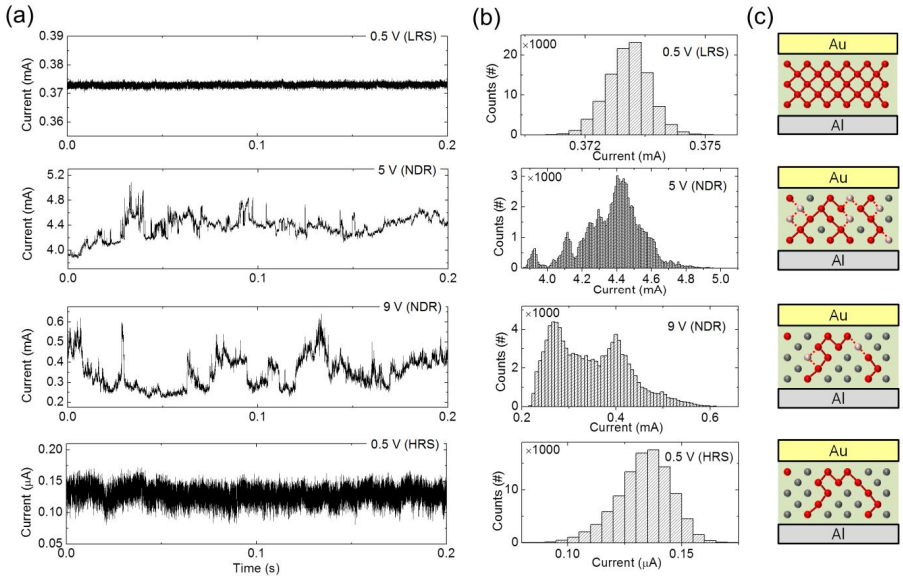


Figure 3.6 (a) The time trace of currents and (b) the corresponding current histograms for a sequence of applying biases of 0.5 V, 5 V, 9 V, and 0.5 V. (c) Schematics explaining the behaviors of each time-dependent current fluctuation. Gray, red, and pink circles represent the unoccupied traps, occupied traps, and unstable traps in which charge trapping-detrapping occur repeatedly, respectively. The red lines represent the current paths formed between occupied traps. The dashed red lines represent the fluctuating current paths due to unstable traps.

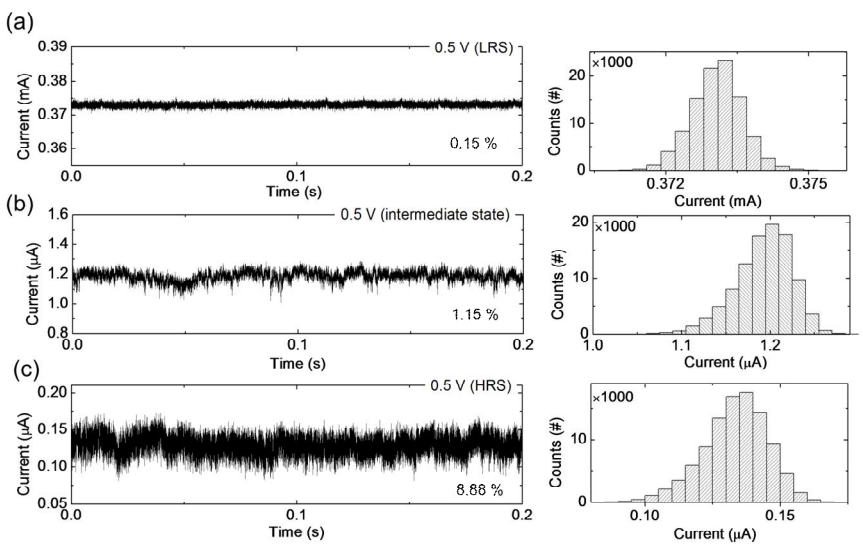


Figure 3.7 Time traces of (a) LRS, (b) IRS and (c) HRS.

The alteration of current traces appears as random telegraph noise (RTN), which is generally explained by trapping and detrapping of charge carriers in the deep trap states [89,107]. Thus, I suggest that the current fluctuation in the NDR is related to the removal of the current pathways *via* the detrapping process of deeply trapped charges (Fig. 3.6(c)). In our discussion, a charge can pass along the charge-occupied deep trap levels, while an electron cannot easily pass through the unoccupied deep traps (Fig. 3.8). In the LRS, most of the deep trap states are occupied, so the most of the conduction process (trapping-detrapping) occur at shallow trap levels. These trapping-detrapping processes are faster (compared to the ones occurring at the deeper traps) and shallow traps are more uniformly distributed over the material. Therefore current paths are more numerous and homogeneously distributed, inducing low noise at low bias (top figure in Fig. 3.6(c)). At higher bias in NDR regime, deeper traps are involved in the conduction process. More deeply trapped charges become unstable and can become detrapped due to the bias-induced lowered trap depth, and the number of current pathways decreases. Thus, the trapping process can occur in the unoccupied trap states, and the trapping-detrapping processes repeat, leading to the fluctuation of number of current pathways (middle two figures in Fig. 3.6(c)). Deep traps are characterized by longer relaxation times (they are so-called long-lived traps), therefore the noise signal resembles the RTN. With the noise gain due to the fluctuation of number of current pathways, $\tilde{S}$ increases, showing $1/f^{1.5}$ noise behaviors related with RTN-like behavior in NDR regime. When the PI:PCBM is in the HRS by turning off the applied bias, the remaining trapped charges are localized, and the trapping-

detrapping process is reduced. At the same time, the current pathways are reduced and their distribution is inhomogeneous, which results in higher RSD in HRS than in LRS (bottom figure in Fig. 3.6(c)).

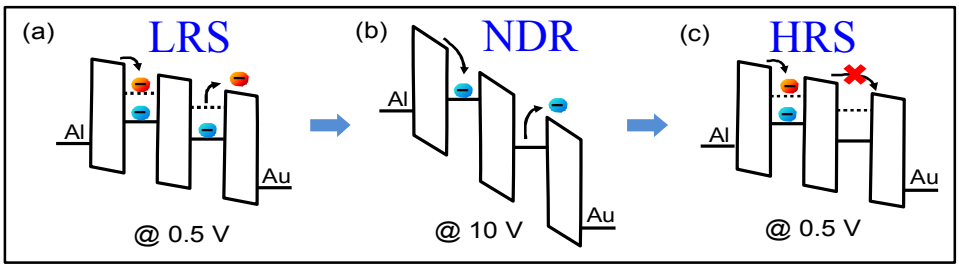


Figure 3.8 Schematics of current pathway removal process with NDR modulation. The red colored charges indicate electrons which are weakly trapped in shallow traps and easily pass along the trap sites. The blue ones indicate electrons which are localized in deep trap states.

3.5. Conductive phase modulation modeling

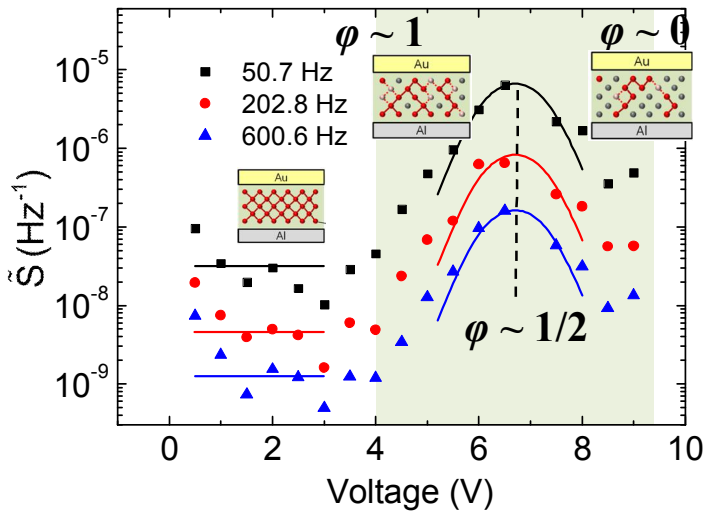


Figure 3.9 The non-monotonic behavior between $\tilde{S}$ and the applied bias.

I also measured the magnitude of $\tilde{S}$ along the applied bias. In Fig. 3.9, a non-monotonic behavior between $\tilde{S}$ and applied bias is presented. In the low bias range (0–4 V) in which *1/f* noise appears, $\tilde{S}$ is almost independent of the applied bias, according to Hooge's empirical relation [4]. On the other hand, in the high bias range (> 4 V) in which the NDR begins and $1/f^{1.5}$ noise appears, a noise peak at ~6 V is observed. This non-monotonic relationship between $\tilde{S}$ and bias is often explained by the charge trapping-detrapping process at the trap states [89,101,108].

The scaling behavior between $\tilde{S}$ and R caused by tuning in the NDR can be explained by the detrapping of charge carriers from deep trap sites due to high bias. The PCBM clusters in the PI matrix [109], the energetic disorder by randomly aligned PI polymers [110], and penetrated aluminum oxide [69] can be attributed to the deep trap formation. Simplifying the dynamics of charge trapping and

detrapping, I can express the rate equation for charge trapping-detrapping as following first-order kinetics, which can be written as [111]

$$\frac{dn^*}{dt} = K_c(n - n^*) - K_t \exp\left[\frac{-\{E_t - \mathrm{E}(V_{app})\}}{k_B T}\right] n^*, \tag{3.5}$$

where E_t is the trap depth measured from the conduction-band edge at zero bias. The trap depth can be varied with PCBM cluster size and local disorder of the PI matrix. I assumed that E_t has a continuous and finite range, such as $E_1 < E_t < E_2$ (here, E_1 and E_2 are the lowest and highest energies of the trap depth, respectively), while $n^* dE_t$ and ndE_t are the densities of filled traps and all the trap sites, respectively, which cover the energy range of (E_t, E_t+dE_t). The first term on the right-hand side of eq.(3.5) is the capture rate of the charges to the unoccupied trap sites from the conduction band. For simplicity, the trapping coefficient (K_c) is considered to be constant because the applied bias in the NDR has a range far beyond the trapping voltage (~2.5 V). The second term on the right-hand side of eq.(3.5) is the detrapping rate of the electrons from the occupied trap sites *via* thermal excitation. The detrapping coefficient is exponentially dependent on E_t – E(V_{app}), which is the effective energy depth of the deep traps with applied bias (V_{app}). Because a higher value of V_{app} will lower the effective energy depth of traps, E(V_{app}) is regarded as a monotonically increasing function with V_{app}. When I apply bias in the NDR region for a sufficient time to reach a steady state, n^* can be expressed as $n^*=n/\{1+(K_t/K_c)\exp[(-E_t+\mathrm{E}(V_{app}))/k_BT]\}$, which is a decreasing function of increasing applied bias. Here, I can consider the ratio of all the filled traps to all the traps as the conductive phase fraction φ. Assuming that E_t is uniform in the range of $E_1 < E_t < E_2$, φ can be written as

$$\varphi = \frac{N^*}{N} = \frac{\int_{E_1}^{E_2} n^* dE_t}{\int_{E_1}^{E_2} n dE_t} = \frac{k_B T}{E_2 - E_1} \mathrm{Log}\left[\frac{e^{E_2/k_B T} + \frac{K_t}{K_c} e^{\mathrm{E}(V_{app})/k_B T}}{e^{E_1/k_B T} + \frac{K_t}{K_c} e^{\mathrm{E}(V_{app})/k_B T}} \right] . \quad (3.6)$$

Here, N^* and N denote the total density of filled traps and trap sites, respectively. In eq.(3.6), φ is a decreasing function, with values in the range between 1 and 0, with increasing V_{app}. Additionally, the variance of the total number of filled traps is known to be $\overline{\Delta N^2} = n_t \varphi(1-\varphi)$; thus, the $\tilde{S}$ in the NDR region can be expressed as $\tilde{S} \propto \varphi(1-\varphi) / f^{1.5}$ [108]. Consequently, when the applied bias reaches a certain voltage where the conductive phase fraction becomes about 1/2, $\tilde{S}$ reaches the maximum value.

To fit the $\tilde{S} \propto \varphi(1-\varphi) / f^{1.5}$ to the NDR region in Fig. 3.9 of the main manuscript, the function E(V_{app}) and the ratio K_t/K_c should be defined. Because a lot of details in PI:PCBM system are veiled, some of system's details need to be assumed. I assume that K_t/K_c can be expressed as K_t/K_c = N_c/n_c = $e^{(ELUMO–EF)/kBT}$ [111] and the Fermi level of polyimide (E_F) is located at the middle of the bandgap of the polymer. The optical bandgap of polyimide cured from BPDA-PPD type polymer was reported to be about 3.10 eV [112], then $E_{LUMO}–E_F$ = 1.55 eV.

E(V_{app}) should represent the magnitude of the decrease of trap level with V_{app}. E(V_{app}) can be approximately determined as the electron energy level difference along the trap. Then E(V_{app}) can be expressed as a linear function, *i.e.*, E(V_{app}) = (trap size/film thickness) × eV_{app} (eV). The PI:PCBM film thickness is about 20 nm

from transmission electron microscope images. And the trap size is assumed to be 2 nm because PCBM molecule size ~1 nm. So I used the function E(V_{app}) = 0.1 eV_{app}.

After that, I fitted the quadratic relation between $\tilde{S}$ and φ to the NDR region (shaded color) in Fig. 3.9. The fitted curve well explains the peak behavior, with values of E_1 and E_2 of 2.07 eV and 2.23 eV, respectively, from the fitted curve. This range of trap energy levels is compatible with the trap energy levels induced by impurities in organic polymers [113].

3.6. Conclusion

In summary, I performed a systematic investigation into the $1/f^{\gamma}$ noise data of PI:PCBM organic nanocomposite memory devices at various biases including within the NDR region. Our data suggest that intermediate resistance switching effects can be of percolative origin, *i.e.*, the modulation of the current distribution *via* trapping-detrapping processes at deep traps. Using a rate equation based on a charge trapping-detrapping in deep traps, I explained how the applied bias can modulate the conductive phase fraction and lead to percolation behavior in the current noise. This work provides insights into how the NDR phenomena in organic nanocomposite system would actually act on the current path formation and its role in the switching mechanism in unipolar resistive memory devices.

Chapter 4. Noise variation with the temperature conditions

4.1. Introduction

Recently, organic material-based nanocomposites have attracted significant attention due to their advantages in the fabrication of low-cost, low-temperature, and solution-processed electronics (such as thin-film transistors, memory devices, solar cells, and wearable sensing components) on large-area flexible platforms [53,57,114–117]. Among these organic electronics, high performance organic resistive memory devices with appropriate architectural designs have been widely studied in the past decade [1,76,118]. The organic nanocomposite resistive memory devices generally show unipolar-type memory characteristics, i.e., the on/off states can be set and reset at the same voltage polarity [1]. In addition, their current-voltage characteristics often show a multi-storage functionality, such as the intermediate resistive states (IRSs), which are typically attributed to a negative differential resistance (NDR) behavior [77,119,120]. Although this phenomenon has been primarily explained by the formation and rupture of conducting filaments in the active layer under a voltage bias or the charge-trapping mechanism, the strongly disordered and inhomogeneous structures have hindered the elaborated understanding of NDR and the IRSs. To exploit the multi-store functionality practically for the higher data density and the low voltage operation, thorough investigations on NDR and its derivative IRSs are necessary.

Under an external electric field, the time- and frequency-resolved current fluctuation information can provide key evidence for the dynamic characteristics of the resistance changes of the active memory layers. The various noise studies have provided a deep insight into the inherent charge transport mechanisms of various disordered systems, such as organic semiconductors, metal-molecule-metal junctions, inorganic filamentary memory devices, and granular systems [85,88–90,101]. In this regard, I have also reported the current noise and the percolative scaling behaviors in an organic nanocomposite memory structure [120].

In this study, for further investigation, the changes of the noise characteristics in a wide range of temperatures were observed in the composite of polystyrene (PS) and phenyl-C61-butyric acid methyl (PCBM). For resistive memory systems which use nanocomposite materials, it is widely known that organic/inorganic nanoclusters embedded in organic matrices can be regarded as the charge trapping elements [55,77,93,94,98,121]. More specifically, the noise scaling behavior from the IRSs and the telegraphic noise in NDR were investigated at a range of temperatures from 80 K to 300 K to observe the electronic dynamics, thereby enabling a better understanding of NDR and the IRSs in organic nanocomposite memory systems. The thermally affected scaling behavior in the IRSs and telegraphic noise in the NDR regime indicated that the multi-level switching and percolation behavior in the organic nanocomposite memory devices were actually controlled by the charge trapping/de-trapping process at the deep trap levels.

4.2. Experimental setup and measurement

For the nanocomposite organic memory material (PS:PCBM), 16 mg of

polystyrene (PS) and 2.5 mg of phenyl-C61-butyric acid methyl ester (PCBM) were dissolved in 2 mL of chlorobenzene. The thermally grown SiO_2 (270 nm thick)/Si substrate was sequentially cleaned with acetone, 2-propanol, and deionized water in sonication for 10 min. Al bottom electrode lines with 100 μm width and 30 nm thickness were deposited using shadow mask patterning. The bottom Al electrodes were exposed to UV-ozone for 10 min to enhance the film uniformity. The prepared nanocomposite memory layer was spin-coated onto the substrate and then annealed on a hot-plate in N_2 at 60 °C for 10 min, followed by exposure of the bottom electrodes using an acetone-soaked swab and then heating at 120 °C for 60 min in N_2. Next, Au top electrodes with 100 μm width and 30 nm thickness were deposited onto the active memory layer. The spin-coated PS:PCBM film was confirmed to be well-blended via photoluminescence measurements (Fig. 4.1). In Fig. 4.1, photoluminescence (PL) spectra were measured on neat PS and PS:PCBM films (0 wt% and 13.5 wt% of PCBM in PS). A 514 nm laser was used as an incidence beam. For only PS, no PL peak was observed in the range between 1.31 eV and 2.28 eV. When PCBM was added to PS, three of PL peaks were observed. As the first sholder peak (1.558 eV) and the middle peak (1.702 eV) were typically observed from neat PCBM film [53], PS:PCBM film was observed to be well blended nanocomposition. Third peak (1.97 eV) at higher PCBM concentration can be related to the photo-induced interaction between PS and PCBM, such as charge transfer [117].

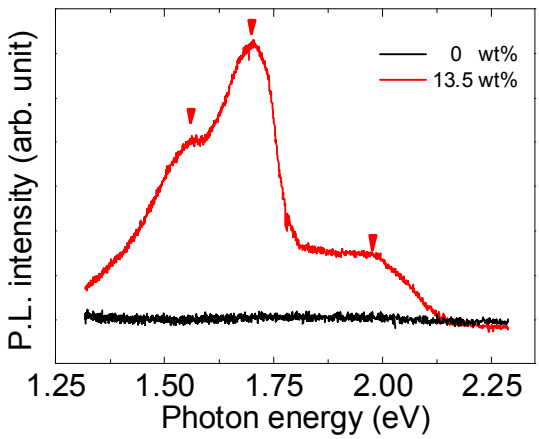


Figure 4.1 Photoluminescence peak of PS film and PS:PCBM film.

The I-V characteristics of the devices were measured using a semiconductor parameter analyzer (Keithley 4200 SCS) and a probe station system (JANIS Model ST-500). For the noise measurement, a spectrum analyzer (Stanford Research SR780) and a ground-isolated 16-bit analog-digital converter (ADC) were used to measure the current noise characteristics in the frequency and time domains, respectively. A battery-powered low-noise current amplifier (Ithaco 1211) was used for converting and amplifying the current noise signal into a voltage signal. A 16-bit digital-analog converter (DAC) was used to apply a voltage bias. A digital multimeter (Agilent 34401A) was used to obtain the average electric current coinciding with the noise power spectral density measurement. All the measurements were performed in a vacuum environment.

Figure 4.2(a) shows the current-voltage (I-V) relation of the PS:PCBM nanocomposite organic memory device. The schematic of the organic memory device and its I-V measurement configuration are also included in the inset. More detailed information for the PS:PCBM material preparation and device

measurement are provided in the Methods section. In the I-V relation, the high resistive states (HRSs) and the low resistive states (LRSs) are presented in both voltage polarities, revealing a good on/off ratio (> 10^5) at the read voltage (|V| < 0.5 V). Usually, the HRS can be switched to the LRS by applying a voltage in the range of 3 V < |V| < 4 V. When |V| is higher than 4 V, the current starts to decrease, which corresponds to NDR. When I turned off the voltage at the stop voltage (V_{stop}) in NDR, the current state returned to the HRS. Notably, the PS:PCBM organic memory showed a unipolar property, even with an asymmetrical electrode structure (Al for the bottom electrode and Au for the top electrode), which suggests that the resistive switching is mainly related to the active material region rather than the interfacial region. The memory devices also showed multi-stable behavior in its I-V characteristics.

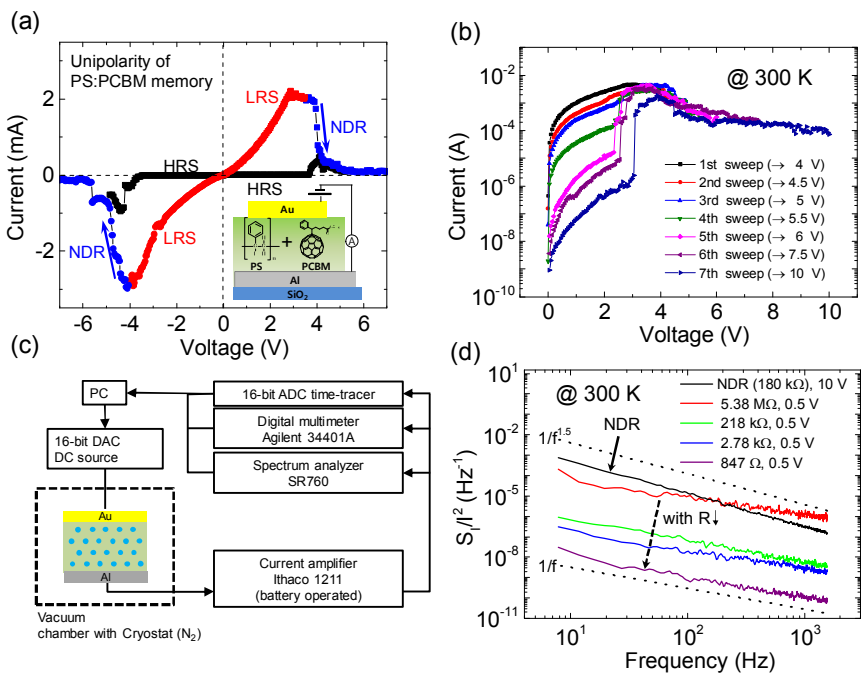


Figure 4.2 Current-voltage (I-V) and noise characteristics of PS:PCBM nanocomposite

memory. **(a)** Unipolar I-V relation of a PS:PCBM nanocomposite memory device. (**b**) I-V characteristics of PS:PCBM exhibiting multi-level resistive states at room temperature. **(c)** Schematic for the noise measurement setup. **(d)** $1/f^{\gamma}$ noise at various resistive states and NDR.

Figure 4.2(b) shows I-V characteristics of the PS:PCBM resistive memory device with multi-level switching behavior. By sweeping the applied voltage from 0 V to V_{stop} and modulating V_{stop}, a number of the IRSs could be approached. The resistive states ranged from 100 MΩ to 1 kΩ. The memory devices also exhibited the multi-stable resistive switching characteristics at low temperature (at 100 K) (Fig. 4.3). Unlike the I-V characteristics at room temperature, however, the number of accesible resistive states was less than at room temperature (at 300 K). This seems to be attributed to the limitation of thermal excitation of trapped charges in deep traps at low temperature.

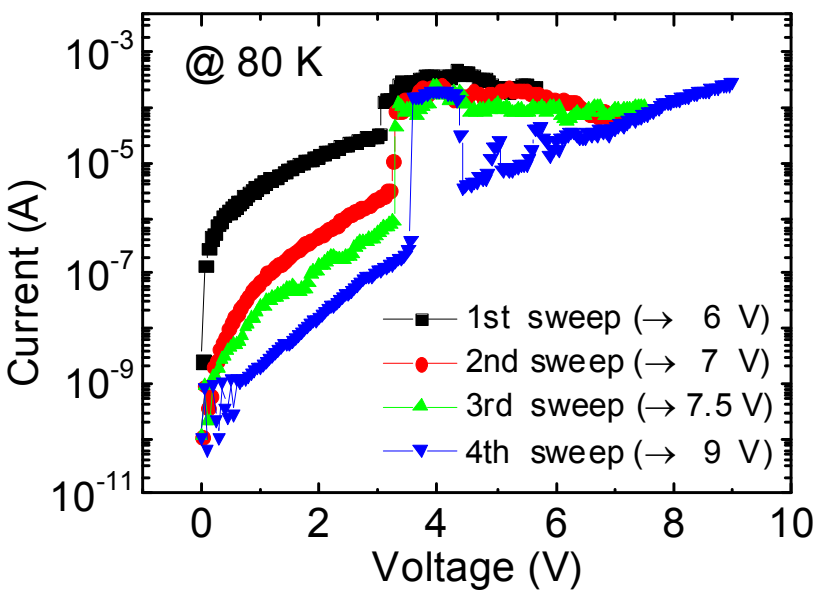


Figure 4.3 Multi-stable I-V characteristics of PS:PCBM memory devices at a low temperature (80 K).

Figure 4.2(c) shows a schematic describing the noise measurement setup. A digital-analog converter (DAC) was used to apply the voltage bias. A battery-powered current amplifier (Ithaco 1211) was used for converting the current noise signal into an amplified voltage signal. An analog-digital converter (ADC) and a spectrum analyzer (SR760) were used to monitor the time domain noise signal and the frequency domain noise signal (power spectral density), respectively. A digital multimeter (Agilent 34401A) was used to simultaneously measure the current and power spectral density. Because the current amplifier has a 50 kHz bandwidth with rise time of 10 μs, I measured low frequency noise in the range from 4 Hz to 1500 Hz in the frequency domain. For the low temperature experiments, a cryostat cooled with liquid nitrogen was used.

Figure 4.2(d) shows the relative power spectral densities for the current signal (S_I/I^2) of our memory device in the IRSs and NDR at room temperature. In the IRSs at a low bias (0.3 V), each resistive state generally showed 1/f type noise in the low frequency region (< 1,500 Hz). In addition, S_I/I^2 decreased as the resistance decreased. On the other hand, at a high voltage (10 V) in NDR, the noise shows $1/f^{1.5}$ type noise (black curve). The different exponent values indicate different current conduction mechanisms present in the IRSs at a low bias and in the NDR regime at a high bias [15,86,120]. Particularly, the exponent value of 1.5 has been understood as a modulation of the local resistances of the material by a diffusing variable such as a local charge carrier density [16,86,122].

4.3. 1/f noise spectra with various temperature conditions

To investigate the thermal effect on electronic noise in the PS:PCBM organic memory device, S_I/I^2 at low temperature was studied at a low bias (0.3 V) in the IRSs and at the high biases (from 6 V to 10 V) in the NDR regime. Figure 4.5(a) and its inset show the relative noise and current level at three different temperature conditions (100, 200, and 300 K). The current level was chosen to be one of the IRSs with low resistance (11.2 kΩ at room temperature). The relative noise (S_I/I^2) was generally $1/f^{\gamma}$, whereas the exponents were $0.9 < \gamma < 1.0$. In Fig. 4.5, relative current power spectral densities at IRSs were measured at low bias (0.5 V) and the different temperatures (80 K, 150 K, 225 K, and 300 K). The noise at low bias showed $1/f^{\gamma}$ noise shape with $0.9 < \gamma < 1.1$ at low frequency (0 Hz < f < 1500 Hz), regardless of temperature.

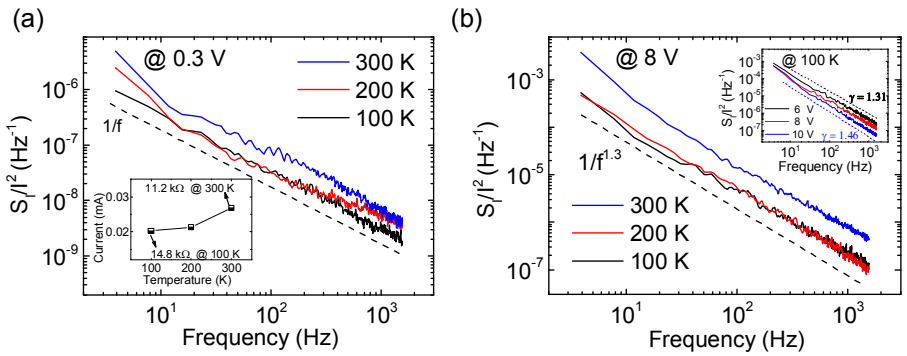


Figure 4.4 Relative power spectral density of PS:PCBM nanocomposite memory at various temperature conditions. (a) The relative power spectral densities at 100 K, 200 K, and 300 K in one of the IRSs. The inset indicates the corresponding current level at 100 K, 200 K, and 300 K. (b) The relative power spectral densities at 100 K, 200 K, and 300 K in the NDR regime (8 V bias). The inset shows the voltage dependence on the relative power spectral density at 100 K.

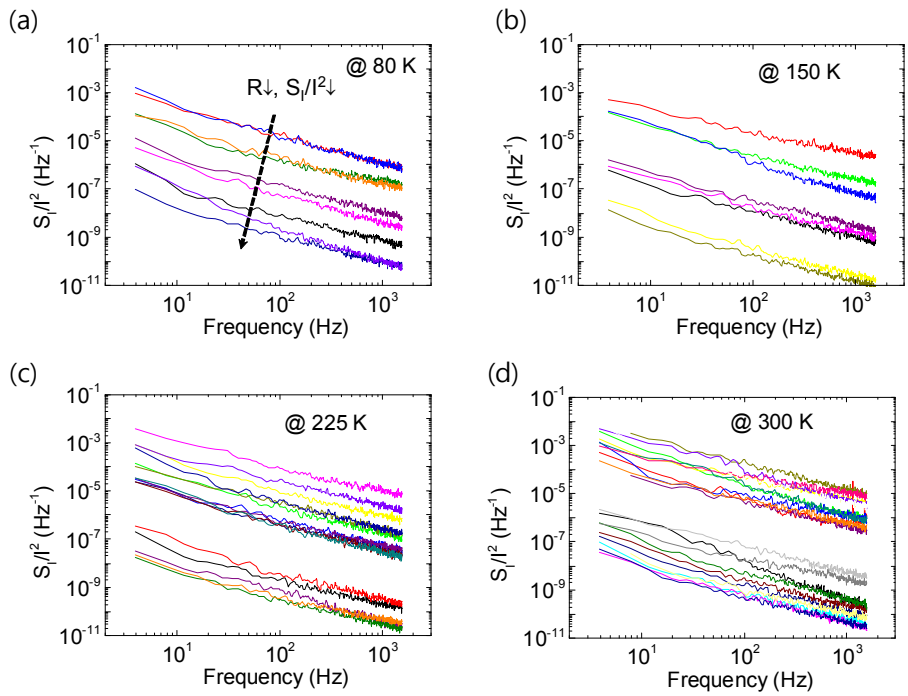


Figure 4.5 1/f noises were observed at various IRSs at low bias (0.5 V) at (a) 80 K, (b) 150K, (c) 225 K, and (d) 300 K.

The relative noise amplitude and the current level were found to decrease as temperature decreased. The magnitude of the relative noise was found to differ 2-3 times between 100 K and 300 K. In addition, the current level slightly decreased as temperature decreased (26.7 μA at 300 K decreased to 20.2 μA at 100 K, inset Fig. 4.4(a)). Figure 4.4(b) shows the temperature dependence on the relative noise in the NDR regime. The $1/f^{\gamma}$ noise with $\gamma > 1.3$ indicated that the noise in the NDR regime can be related with the discrete current levels caused by the trapping and de-trapping of charge carriers and the contribution of the diffusion process [19,122,123]. Note that the superposition of Lorentzian noise caused by traps with the characteristic time distribution can show $1/f^{\gamma}$ with $\gamma = 1 \pm 0.3$ [19]. In our PS:PCBM memory device at an 8 V bias, the relative noise maintained 1/f

noise with $\gamma \sim 1.3$. In addition, approximately 3 times lower relative noise was observed at 100 K and 200 K than at 300 K. By varying the voltage in the NDR regime, I also observed that γ increased with increasing voltage from 1.31 (at 6 V) to 1.46 (at 10 V) (inset of Fig. 4.4(b)). The increase of γ can be explained by the domination of trapping/de-trapping processes in deep trap levels with a higher voltage bias [120].

4.3.1. Scaling behavior variation

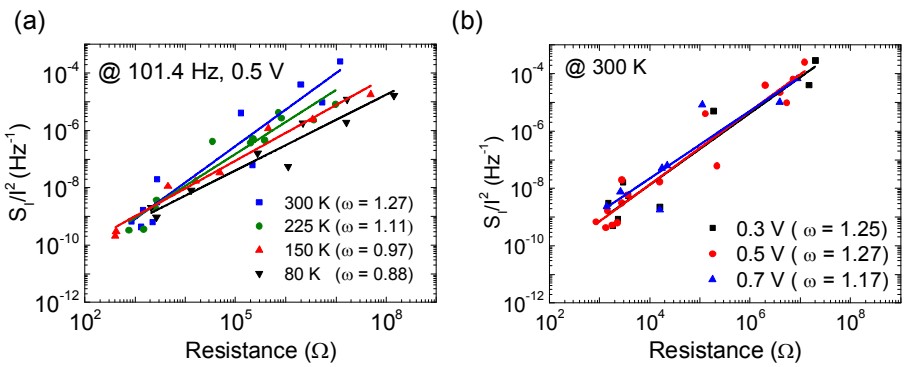


Figure 4.6 (a) Power-law relationships between the relative power spectral densities and the resistance of the IRSs at 80 K, 150 K, 225 K, and 300 K with f = 101.4 Hz and 0.5 V bias. (b) Power-law relationship between the relative power spectral density and the resistance of the IRSs at 0.3 V, 0.5 V, and 0.7 V at 300 K with f = 101.4 Hz.

As mentioned above, by setting a higher V_{stop}, the IRSs with higher resistance can be approached, as the current pathways with a reduced conductivity are fixed (various IRSs shown in Fig. 4.2(b)). Thus, the voltage bias modulation in NDR can lead to the various resistive states by current pathway deformation and fluctuation. These current pathways could be identified as conductive filaments, such as metal ion inclusions or phase transition of the active layer [85,91]. However, the nonlinear (non-ohmic) and the unipolar I-V relation of the PS:PCBM memory

device was not consistent with those arguments; rather, the I-V characteristic indicates that the current pathways are related to the conduction along trap-free (or trap-filled) regions. These various current pathways for each IRS can be regarded as a current distribution through the resistance network of a percolation system. Because traps play the part of current bridges, the trap sites can be considered to be elementary bonds or sites in a percolation theory.

To investigate the relationship between S_I/I^2 and R, each IRS was approached by modulating V_{stop} at the NDR regime, and then the power spectral density and average current were measured simultaneously. I examined the relationship between the S_I/I^2 and R by varying both the temperatures and the voltage biases. Figure 4.6(a) shows that PS:PCBM organic memory devices exhibit a scaling behavior between the relative power spectral density and resistance. As the temperature decreases from 300 K to 80 K, ω was observed to decrease from 1.27 to 0.88. A similar ω value (1.22) at 300 K was also observed from other devices. The ω value of the PS:PCBM memory device for 300 K can be comparable to ω = 0.95 measured for the polyimide (PI):PCBM organic nanocomposite memory device at room temperature in the previous study [120]. Although PCBM concentration, monomer type, and degree of polymerization are different between PS and PI, both PS:PCBM and PI:PCBM showed similar resistive switching and noise characteristics. The minor difference of ω between PS:PCBM and PI:PCBM is attributed to the geometrical differences of the trap distribution and the energy disorder between the polymers and PCBM. Note that ω = 1.8 was reported for a conductive filament type nickel oxide resistive memory device at room temperature [85]. The relative noise in the LRS, which has abundant current

pathways, was not significantly affected by the temperature conditions. In contrast, the relative noise in the HRS, which lacks current pathways, was greatly changed by the temperature conditions, showing over a 10^2 magnitude difference between 300 K and 80 K.

The change of ω at different temperature conditions can be attributed to the geometrical variation of the current pathways. From a relation between electrical current and mobility ($I \propto qN\mu$), fluctuations in the electrical current can be written as $\delta I \propto q(\delta N)\mu + qN(\delta\mu)$, where q is the charge of a charge carrier, N is the number of charge carriers, and μ is the mobility. Accordingly, mobility fluctuation ($\delta\mu$) and number fluctuation (δN) have been considered as the sources of 1/f noise [19,123,124]. Mobility fluctuation is primarily caused by charge scattering, and number fluctuation is determined by capture or emission of electrons at trap/scattering centers. Although the major source for the 1/f noise in PS:PCBM is uncertain here, I can explain the lower ω at low temperature with both mobility and number fluctuations. If the number of current pathways is lower at the higher resistive state, then the pathways for charge transport are more limited and become thinner. Charge carriers with higher thermal energy would undergo surface scattering (mobility fluctuation) in the thin current pathway because charge carriers in organic polymers have longer inelastic mean free path at higher temperature [125,126]. If the width of the current pathway gets thinner, surface scattering would occur more frequently. On the other hand, charge carriers with higher thermal energy would be more likely to be captured/emitted at shallow trap centers (number fluctuation). In any case, the geometrical formation of current pathways is important in the different scaling behaviors at the different

temperatures. Meanwhile, ω was unchanged under varying low bias voltages at room temperature (Fig. 4.6(d)), indicating that the resistance fluctuation in the PS:PCBM percolating network remains the same under different voltage biases, i.e., the scaling behavior is induced by purely geometrical formation of current pathways in the low bias range [85].

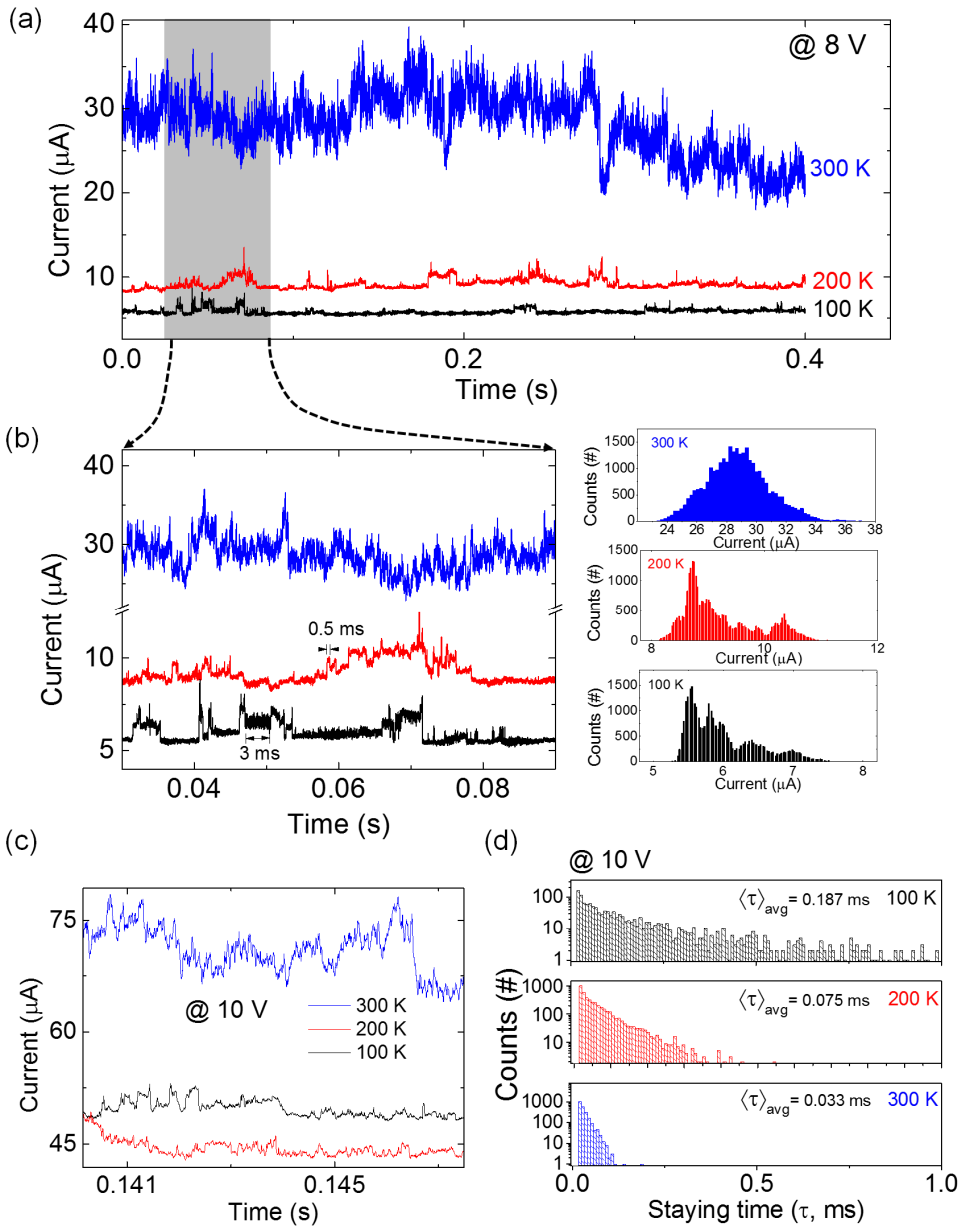


Figure 4.7 Telegraphic noise of PS:PCBM nanocomposite memory at NDR. Time traces of currents at 100 K, 200 K, and 300 K in the NDR regime (8 V bias) for (a) 0.4 s and (b) 50 ms. The right inset in (b) is the corresponding current histograms at 100 K, 200 K, and 300 K time traces for 50 ms. (c) Time traces of the currents at 100 K, 200 K, and 300 K at 10 V bias and (d) distribution of the dwell times for telegraphic noise at 100 K, 200 K, and 300 K with 10 V bias.

4.4. Telegraphic noise variation

4.4.1. Temperature and voltage effect on telegraphic noise

I studied the time domain signal of noise in NDR with varying temperatures from 100 K to 300 K. In the low bias regime where 1/f noise is found (< 1 V), the time trace data showed a single peak distribution of current values. In the NDR regime (> 4 V), however, the time trace signal usually exhibited alterations of the current levels, which can be called telegraphic noise (Fig. 4.7). At the bias of 8 V in the NDR regime, the time trace data were measured at 100 K, 200 K, and 300 K. At 300 K, the current noise showed a large fluctuation with a magnitude of approximately 10 μA. In contrast, the fluctuating noise was drastically reduced and showed longer dwell times at 200 K and 100 K. In addition, the noise at 300 K showed alternating current plateaus with a much shorter dwell time of approximately tens of microseconds (see Supplementary Fig. 4.8).

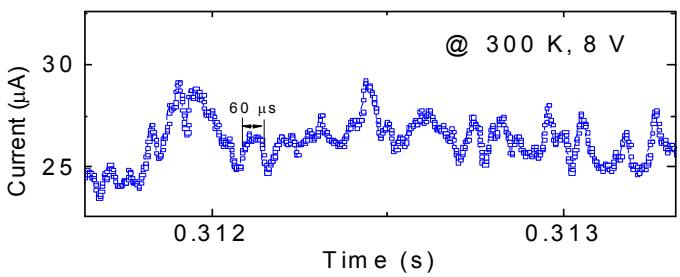


Figure 4.8 Time trace of current at 300K in the NDR regime (8 V) for 2 ms.

The histogram graphs at the right of Fig. 4.7(b) indicate the distribution of current values within 60 ms at the temperatures of 100 K, 200 K, and 300 K. At 300 K, because the characteristic time for the current plateaus transition was too small, the distribution of current values appeared to have one peak. As the temperature decreased to 200 K and 100 K, several distinct peaks could be

observed in the current distribution. Compared with the time traces for 200 K and 100 K, the data for 100 K showed a much longer dwell time of the current level transition.

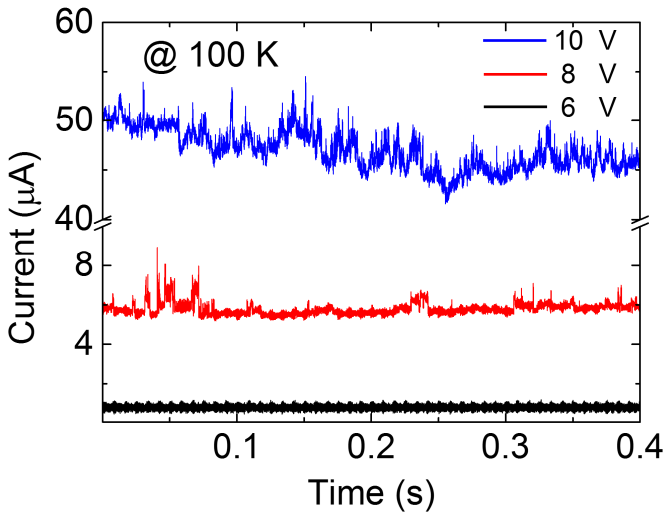


Figure 4.9 Time traces of currents at 6 V, 8 V, and 10 V in 100 K for 0.4 s.

If the switching mechanism of PS:PCBM resistive memory originates from trap sites, the telegraphic noise would be affected by not only temperature, but also by an applied voltage bias, because the applied voltage bias will give an influence on the trapping/de-trapping process by the lowered trap barrier. In result, the telegraphic noise at NDR was also affected by the applied voltage, as the increasing voltage led to more frequent current level transitions at 100 K (Fig. 4.9). At 100 K, the large telegraphic fluctuation was observed in PS:PCBM memory devices as increasing the voltage from 6 V to 10 V. Thermal excitation of charges trapped in the deep trap levels was not enough at 6 V for the overcoming the trap barrier. As increasing the voltage to 10 V, otherwise, thermal excitation was high enough to overcome the trap barrier, resulting in the telegraphic noise.

Usually, two-level random telegraph noise is characterized by estimating the characteristic times of capture/emission [44,127]. However, because the telegraphic noise of the PS:PCBM memory device showed an alternation in the multiple current states, I estimated the representative dwell time of this telegraphic noise as the average of all the dwell times (τ) for which current states maintain. I measured the telegraphic noise with a bias of 10 V at various temperature conditions (Fig. 4.7(c)). Because the telegraphic noise at 10 V showed a shorter dwell time than that at 8 V, an adequate amount of τ sampling could be achieved. Then, to evaluate the change of the average of the dwell times ($\langle\tau\rangle_{avg}$) in the temperature conditions, I measured τ and plotted the distribution on a semi-log scale (Fig. 4.7(d)). In Fig. 4.7(d), the flections at the border of different slopes of the distributions were observed at 100 K and 200 K. These flections can be attributed to the contributions of different characteristic times of traps which are major noise sources in the time traces. $\langle\tau\rangle_{avg}$ decreased as the temperature increased, with values of 0.187 ms, 0.075 ms, and 0.033 ms for 100 K, 200 K, and 300 K, respectively. Here, the longer dwell times at lower temperature and the lower voltage bias indicate that the noise was induced by a voltage driven and thermally activated trapping/de-trapping process at the deep trap levels [42].

4.4.2. Reversible access of current states

Figures 4.10(a) and 4.10(b) show six of the well-separated current plateaus at the bias of 6 V at 200 K. These current plateaus have a nearly regular current interval of approximately 0.3 μA. Each current plateau was reversibly accessible

during the discrete current alteration process. This reversible access of current states indicates that the telegraphic noise occurs in the stationary structure. For a number of traps n, the number of current states can be 2^n [127]; thus, at least 3 traps contributed to the random telegraphic noise, as shown in Fig. 4.10(a). To better visualize the dynamics of the transition between the current states, the behavior is shown in a time lag plot (TLP) [43,128]. Note that a TLP is a simple but effective analysis method for understanding both the complex waveforms and the statistical behaviors of telegraphic noise. A TLP can be drawn by plotting points on a 2-dimensional graph, where the x- and y-axis are set to the current value at time t and $t+\Delta t$, respectively; one can track the transitions between the current states from this dragging feature (Fig. 4.10(c)). For our study, I set Δt = 50 μs because the transition time was estimated to be 10-20 μs. Figure 4.10(d) shows the TLP for the data of Fig. 4.10(a). For the diagonal element, six current states were observed, as shown in the raw time trace (Fig. 4.10(a)). The non-diagonal points indicate the transition between current states, i.e., the upper points indicate the transition from the lower current state to the higher current state and vice versa.

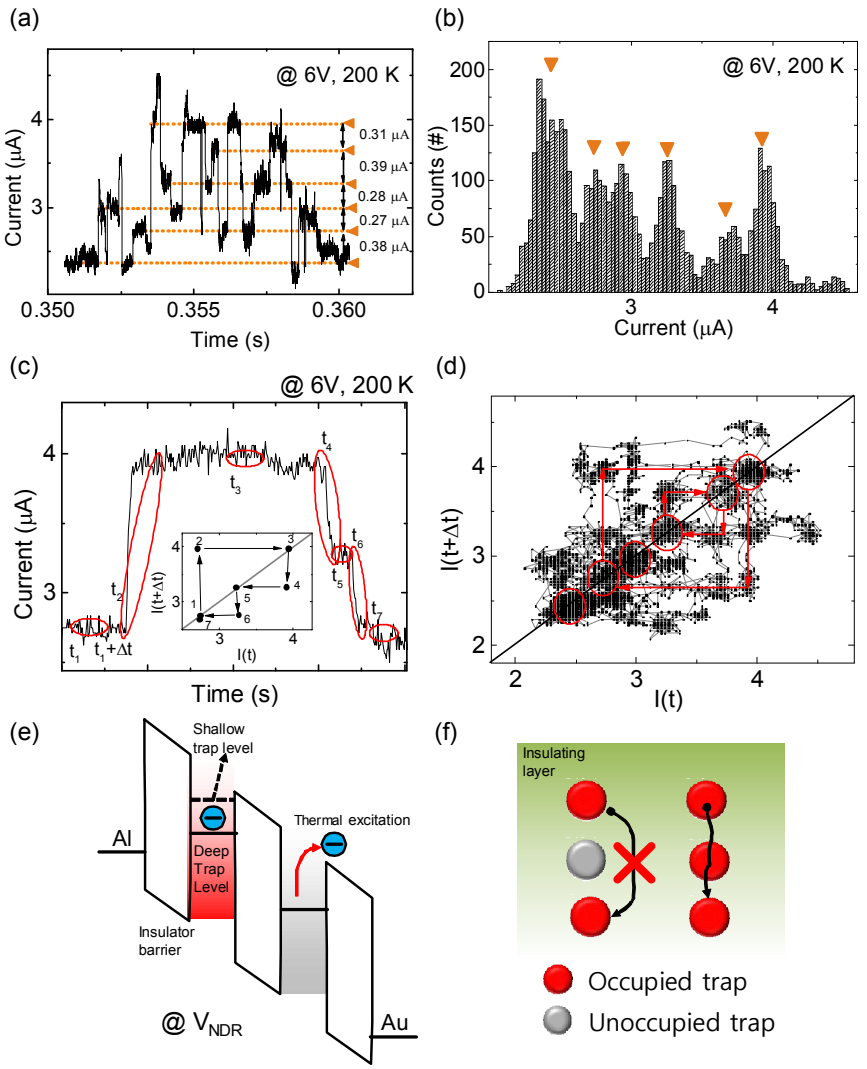


Figure 4.10 Reversible access of the resistive states and schematics of the current pathway formation and removal process. (a) Well-separated current plateaus at 6 V bias and 200 K and (b) the corresponding current histogram. (c) Explanation of the Time Lag Plot (TLP). (d) TLP of (a). (e) Schematic of the current pathway removal process with NDR modulation. The blue colored circles indicate the electrons that are localized in the deep trap levels or escaping the deep trap levels. (f) Schematic of current pathway formation and removal by the charge trapping/de-trapping at the deep trap levels.

The telegraphic noise shown in the PS:PCBM organic nanocomposite memory device can be understood as the current paths fluctuation induced by charge

trapping and de-trapping in the deep trap levels distributed in the organic polymer. A schematic illustrating the current pathway formation is presented in Fig. 4.10(e). The white boxes indicate the gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) of the insulating matrix (PS). As the trap centers are distributed in the insulating matrix, charge carriers can be trapped and localized in the deep trap energy levels due to a high trap energy barrier relative to the conduction level of the insulating matrix. If the deep trap levels are already occupied by charge carriers, charge carriers can easily pass through the shallow trap levels above the deep trap levels *via* trap-assisted tunneling or the Poole-Frenkel conduction process (Fig. 4.10(f)) [120,129]. As a result, the neighboring traps with the occupied deep trap levels can form a current pathway. At the high voltage bias, charge carriers trapped in the deep trap levels can be unstable and detrapped due to the lowered trap barrier and thermal excitation. When the deep trap level is unoccupied, the current pathway between traps is cut off. If the unoccupied deep trap levels are reoccupied, the current pathways can be reformed. Thus, the telegraphic noise in the NDR regime can be understood as the fluctuation of the current pathways due to the trapping/de-trapping process at the deep trap levels. Due to the energy distribution of the deep trap levels in the PS:PCBM layer [120], more charge carriers in the deeper trap levels would be unstable as the higher bias is applied, resulting in a decrease in the number of current pathways. Furthermore, the exponent value of 1.5 at the high voltage bias in Fig. 4.2(d) can be explained by the diffusion process caused by a gradient of the local number density of charge carriers trapped in the deep trap levels.

4.5. Conclusion

In summary, I present the noise characteristics of the organic nanocomposite (PS:PCBM) memory under various temperature conditions. The geometrical formation of constricted current paths can exhibit percolation behavior in the form of $S_I(f)/I^2 \propto R^{\omega}$. The suppression and clear appearance of the telegraphic noise in NDR at low temperature indicates that the charge trapping/de-trapping process at the traps is the principal cause of NDR, and this process results in the intermediate resistive states at low voltage bias via the current pathway formation. The trap formation and distribution in the nanocomposite resistive memory device system will be important in next-generation resistive memory devices; this study will provide a better understanding of resistive memory devices and promote the development of more practical and sophisticated resistive memory devices.

Chapter 5. Summary

In this thesis, I present our research on organic resistive memory devices regarding the fabrication and switching/transport mechanism perspective. First, I demonstrated 4K-bit and microscale integration of organic resistive memory devices using orthogonal photolithography method. Using fluorinated photoresist, the resulting memory devices were not damaged from the photolithography process, maintaining excellent memory property and device yield. For other study on switching/transport mechanism of the organic resistive memory devices, I performed noise measurement and analysis on the memory devices. From the scaling behavior between 1/f noise and resistance within IRSs, I concluded that IRSs are consisted of distribution of localized current pathways. From the telegraphic noise in NDR and the temperature variable experiment on them, I concluded that trapping/detrapping process dominates in NDR and NDR result in IRSs by sweeping out the trapped charges in deep trap levels. In other words, the connection of deeply occupied traps are convincing candidate for the localized current pathways.

Appendices

Appendix A All I-V curves of operative 4K-bit and microscale organic memory devices. (Related with Chapter 2)

I measured a total of 245 memory cells out of 64 × 64 = 4096 cells. Figure A1-A3 summarizes the I-V curves measured from selected 175 cells. Figure A1 shows the schematic indicating locations of some measured cells. The I-V curves are provided in Figs. A2 and A3. The panels with blue and green background indicate operative memory cells whereas the panels with grey background indicate inoperative memory cells.

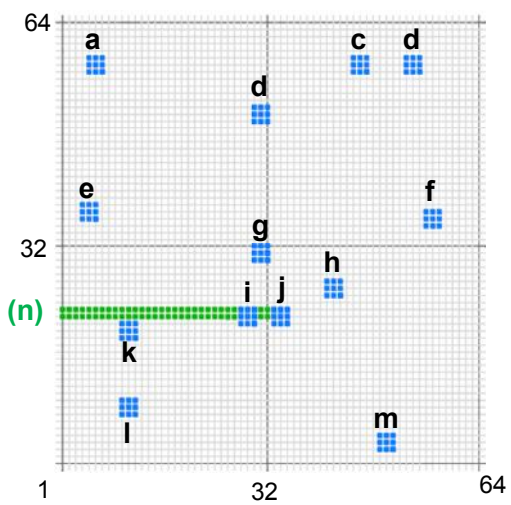
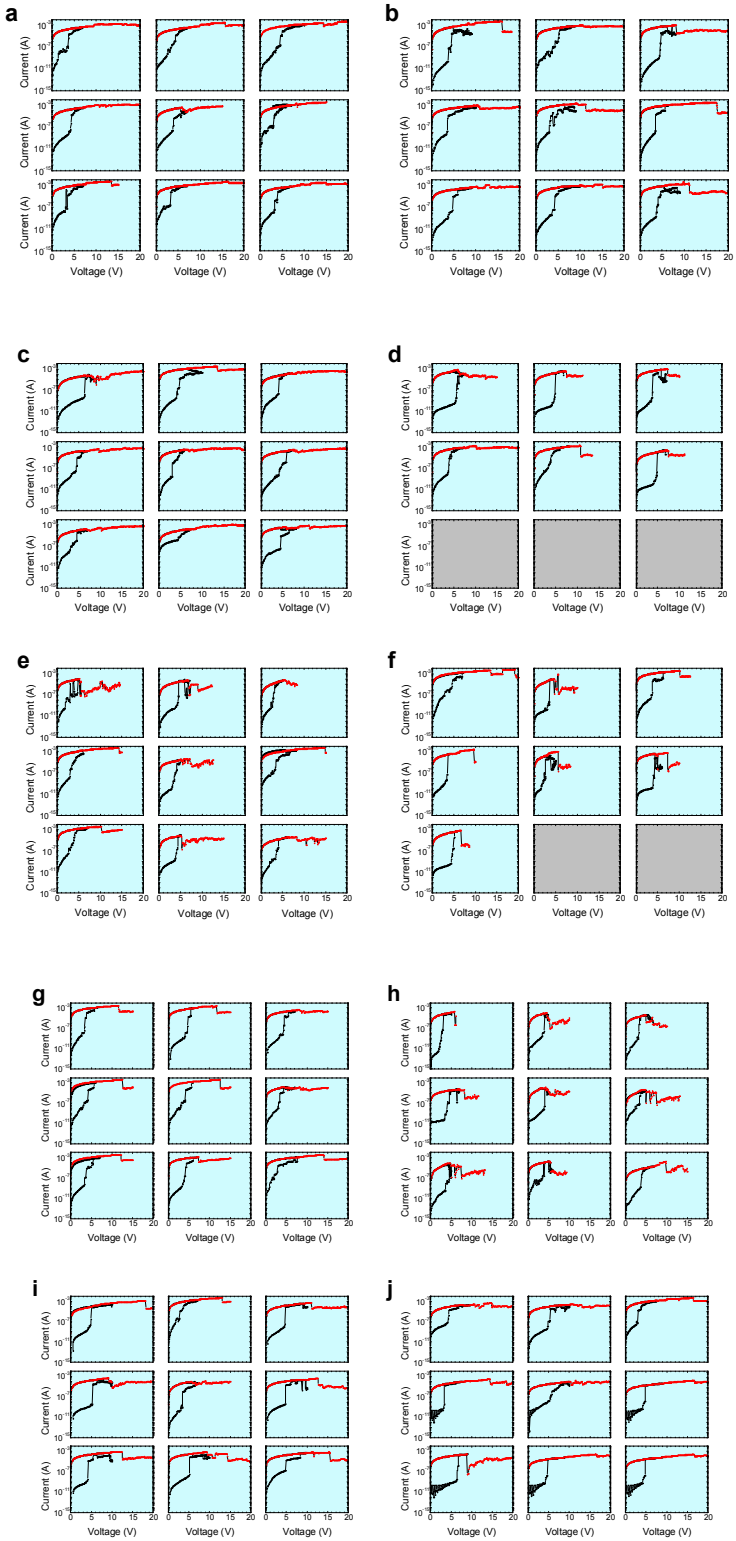


Figure A1 The schematic indicating the selected regions for measuring the memory cells from 4k-bit memory array.


a
b
c
d
e
f
g
h
i
j
Current (A)
Voltage (V)

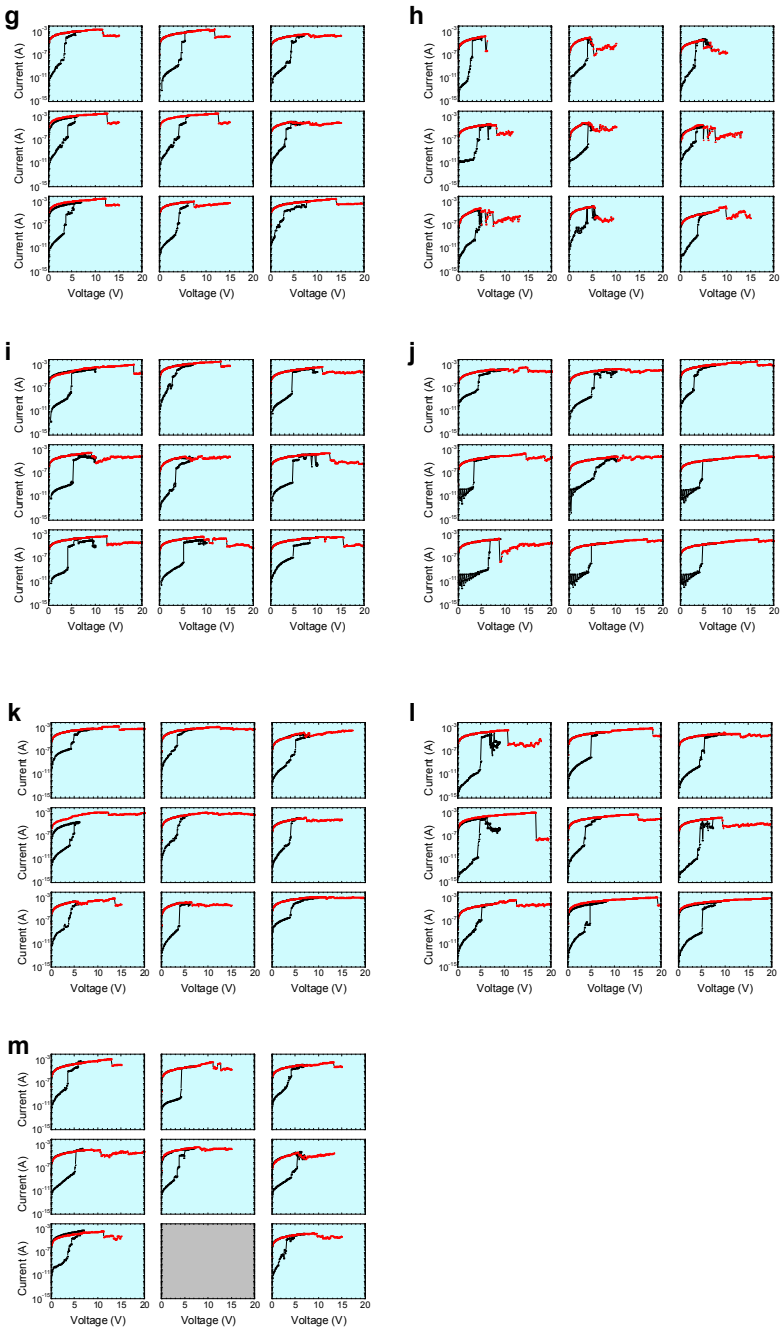


Figure A2 I-V curves of the organic memory cells in regions **a** - **m** in Fig. A1.

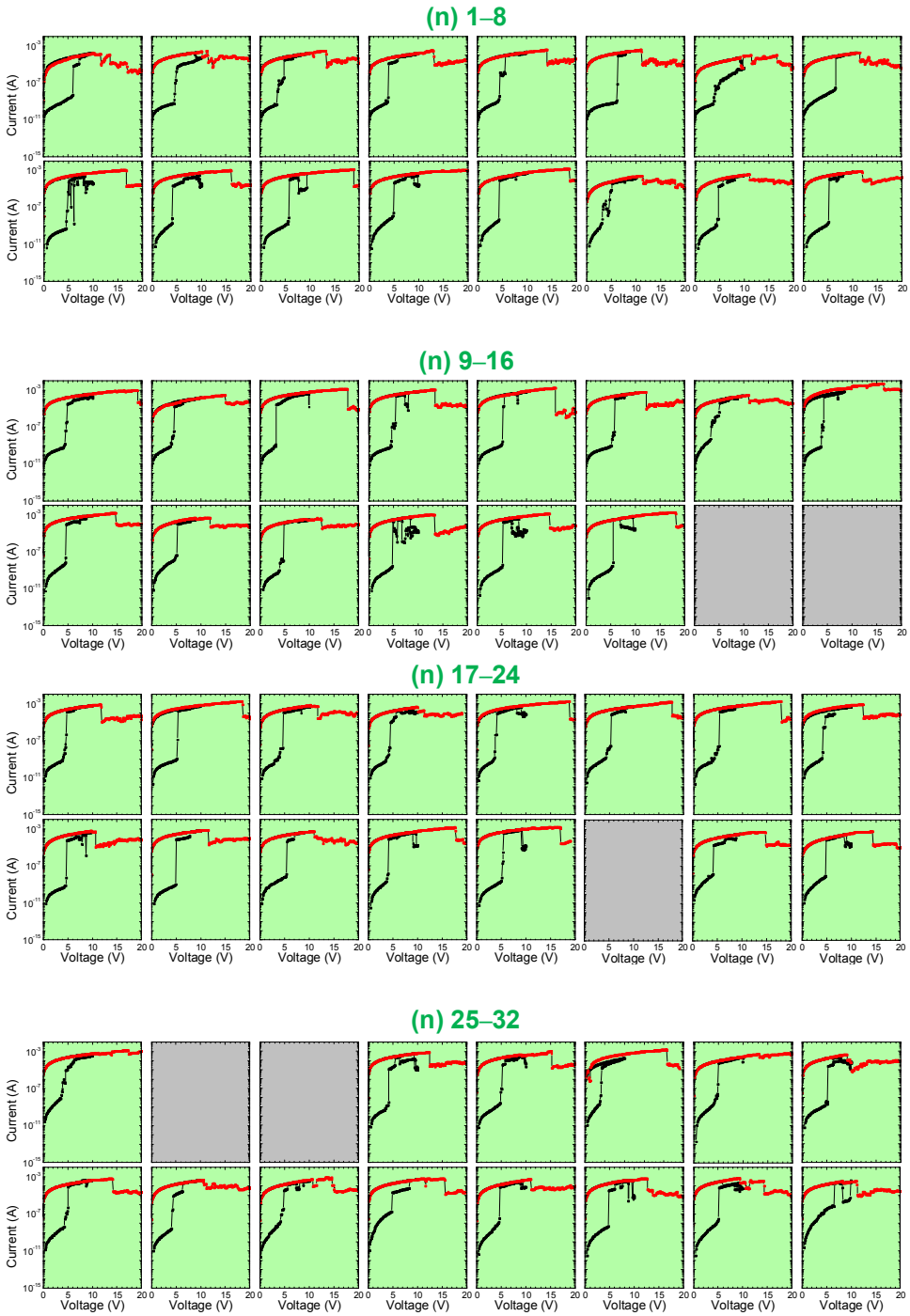


Figure A3 I-V curves of the organic memory cells in regions (**n)** in Fig. A1.

Appendix B Additional explanation for 1/f noise with exponent 1.5 in NDR (Related with Chapter 3, Chapter 4)

The exponent value of 1.5 has been explained as ion diffusion/drift noise in a deformation of conductive filaments for inorganic resistive memory devices [16,86]. In a theoretical approach, the diffusion noise can arise in a percolation network if the resistance (r) of a small but macroscopic piece of the material is modulated by a diffusing variable like the local number density (n) (i.e., $\delta r = (dr / dn)\delta n$) [122]. This statement can also be applied to our discussion about the current paths fluctuation induced by trapping/de-trapping in the deep trap levels. At the high voltage bias, charge carriers trapped in the deep trap levels become unstable due to a lowered trap barrier and they can move to neighboring deep trap levels. If there is a gradient of the number density ($N(\mathbf{r},t)$) of charge carriers trapped in the deep trap levels, $N(\mathbf{r},t)$ would be changed over time according to a diffusion process of charge carriers trapped in the deep traps ($\frac{\partial N(\mathbf{r},t)}{\partial t} = D\nabla^2 N(\mathbf{r},t)$, where D is a diffusion coefficient.). This diffusion process would induce the local resistance modulation because the occupied deep trap levels can form the current pathways.

In our study, the telegraphic noises were only observed in 1/f$^{\gamma}$ noise with the exponent values of 1.3-1.5 at the high voltage bias (in the NDR regime). If only

two-level transitions were observed in our time trace data, a Lorentzian power spectrum should be observed. However, as our manuscript shows in Figure 3, I observed the transitions between the multiple current levels in time domain. This phenomenon can be explained as a result of multiple traps with different trapping/de-trapping characteristic times. Therefore, the superposition of the Lorentzian noises caused by each traps is possible in frequency domain. From the expression for a superposition of individual Generation-Recombination noise sources with the life time distribution [123] (The expression is, $S_N(\omega) = \overline{4\delta N^2}\int_{\tau_1}^{\tau_2} g(\tau_N)\frac{\tau_N}{1+(\omega\tau_N)^2}d\tau_N$), if the lifetime is distributed on a logarithmically wide time scale between τ_1 and τ_2 ($g(\tau_N) = [\tau_N \ln(\tau_1/\tau_2)]^{-1}$), the power spectrum density would follow 1/f noise but limited by τ_1 and τ_2. If $\omega \gg 1/\tau_1$, $1/f^2$ noise would be observed in frequency domain. In our study, the exponent values from 1.3 to 1.5 in the low frequency range (< 1500 Hz) are reasonable with a deviated characteristic time distribution from the logarithmic distribution. As I focused on the low frequency noise (< 1500 Hz) in our sample, it is possible that $1/f^2$ noise can be observed at higher frequency. Because the exponent value larger than 1.3 was observed at the high voltage bias in the NDR regime, the contribution of diffusion noise would be considerable.

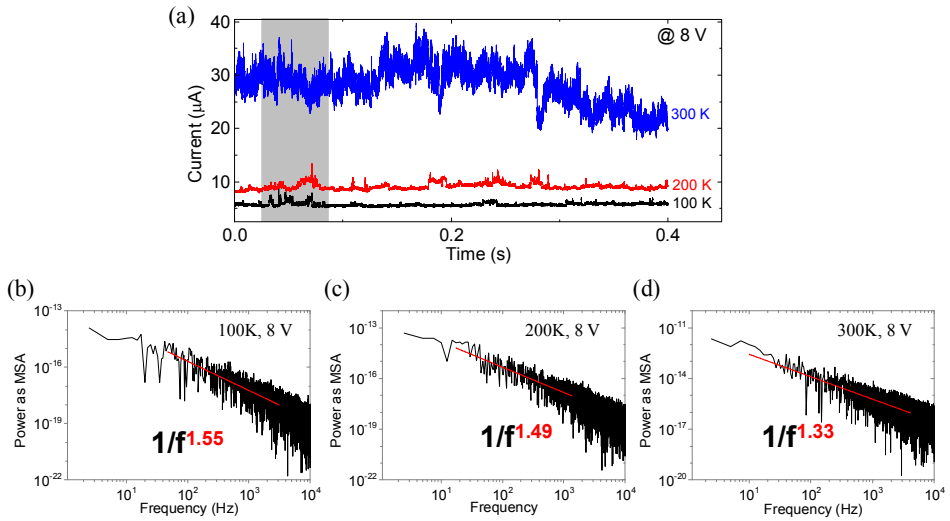


Figure B1 (a) Time traces of currents at 100 K, 200 K, and 300 K in the NDR regime at 8 V bias. MSA values at (b) 100 K, (c) 200 K and (d) 300 K.

I directly estimated mean squared amplitude (MSA) from the time traces using a fast Fourier transform in Origin software, where MSA corresponds to power spectral density (Fig. B1). Note that these estimations were performed in the same time traces which were used in our original manuscript. From Fig. B1, the exponent values of 1.55, 1.49 and 1.33 were extracted in the low frequency range (0 – 2000 Hz) at 100 K, 200 K and 300 K at 8 V bias. Although 1.55 and 1.49 are slightly deviated from 1.3 in Fig. 4.4, this deviation is acceptable in our discussion as the power spectral density values were averaged over 150 spectra in the SR760 spectrum analyzer.

References

[1] B. Cho, S. Song, Y. Ji, T. W. Kim, and T. Lee, *Adv. Funct. Mater.* **21**, 2806 (2011).

[2] B. A. A. Zakhidov, J. Lee, H. H. Fong, J. A. Defranco, M. Chatzichristidi, P. G. Taylor, C. K. Ober, and G. Malliaras, *Adv. Mater.* **20**, 3481 (2008).

[3] J. Lee, M. Chatzichristidi, A. A. Zakhidov, P. G. Taylor, J. A. Defranco, H. S. Hwang, H. H. Fong, A. B. Holmes, G. G. Malliaras, and C. K. Ober, *J. Am. Chem. Soc.* **130**, 11564 (2008).

[4] S. Kogan, *Electronic Noise and Fluctuations in Solids* (Cambridge Univ. Press, 2008).

[5] C. Surya and T. Y. Hsiang, *Phys. Rev.* B **33**, 4898 (1986).

[6] C. T. Sah and F. H. Hielscher, *Phys. Rev. Lett.* **17**, 956 (1966).

[7] F. M. Klaassen, *IEEE Trans. Electron Devices* **18**, 887 (1971).

[8] M. Stoisiek and D. Wolf, *IEEE Trans. Electron Devices* **ED-27**, 1753 (1980).

[9] J. Rhayem, D. Rigaud, M. Valenza, N. Szydlo, and H. Lebrun, *Solid. State. Electron.* **43**, 713 (1999).

[10] L. Ke, X. Y. Zhao, R. S. Kumar, and S. J. Chua, *IEEE Electron Device Lett.* **27**, 555 (2006).

[11] S. Bychikhin, D. Pogany, L. K. J. Vandamme, G. Meneghesso, and E. Zanoni, *J. Appl. Phys*. **97**, 123714 (2005).

[12] L. K. J. Vandamme, R. Alabedra, and M. Zommiti, *Solid. State. Electron.* **26**, 671 (1983).

[13] L. Jiang, E. R. Nowak, P. E. Scott, J. Johnson, J. M. Slaughter, J. J. Sun,

and R. W. Dave, *Phys. Rev. B* **69**, 54407 (2004).

[14] S. Bae, J.-H. Lee, H. Kwon, J. Ahn, J. Om, C. H. Park, and J. Lee, *IEEE Trans. Electron Devices* **56**, 1624 (2009).

[15] J. K. Lee, H. Y. Jeong, I. T. Cho, J. Y. Lee, S. Y. Choi, H. I. Kwon, and J. H. Lee, *IEEE Electron Device Lett.* **31**, 603 (2010).

[16] N. Raghavan, D. D. Frey, and K. L. Pey, *Microelectron. Reliab*. **54**, 1729 (2014).

[17] Z. Fang, H. Y. Yu, J. A. Chroboczek, G. Ghibaudo, J. Buckley, B. De Salvo, X. Li, and D. L. Kwong, *IEEE Trans. Electron Devices* **59**, 850 (2012).

[18] D. Lee, J. Lee, M. Jo, J. Park, M. Siddik, and H. Hwang, *IEEE Electron Device Lett.* **32**, 964 (2011).

[19] F. N. Hooge, *IEEE Trans. Electron Devices* **41**, 1926 (1994).

[20] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, *Reports Prog. Phys*. **44**, 479 (1981).

[21] F. N. N. Hooge, *IEEE Trans. Electron Devices* **41**, 1926 (2004).

[22] R. F. Voss, *J. Phys. C Solid State Phys*. **11**, L923 (1978).

[23] R. F. Voss, *33rd Annu. Symp. Freq. Control.* 1979 40 (1979).

[24] P. Dutta and P. M. Horn, *Rev. Mod. Phys.* **53**, 497 (1981).

[25] A. L. McWhorter, *1/f noise and related surface effects in germanium*, phD dissertation, MIT, Cambridge, MA, (1955).

[26] F. N. Hooge, Phys. Lett. A **29**, 139 (1969).

[27] F. N. Hooge, Phys. B+C **83**, 14 (1976).

[28] L. K. J. Vandamme, *2013 22nd Int. Conf. Noise Fluctuations*, ICNF 2013 (2013).

[29] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, *Phys. Stat. Sol.* **124**, 571 (1991).

[30] K. K. Hung, P.-K. Ko, C. Hu, and Y. C. Cheng, *IEEE Trans. Electron Devices* **37**, 654 (1990).

[31] M. J. Uren, D. J. Day, and M. J. Kirton, *Appl. Phys. Lett.* **47**, 1195 (1985).

[32] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, *IEEE Electron Device Lett.* **11**, 90 (1990).

[33] R. Soni, P. Meuffels, A. Petraru, M. Weides, C. Kügeler, R. Waser, and H. Kohlstedt, *J. Appl. Phys*. **107**, 024517 (2010).

[34] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, *IEEE Trans. Electron Devices* **61**, 2920 (2014).

[35] C. Dekker, A. J. Scholten, F. Liefrink, R. Eppenga, H. van Houten, and C. Foxon, *Phys. Rev. Lett.* **66**, 2148 (1991).

[36] D. Lachance-Quirion, S. Tremblay, S. A. Lamarre, V. Méthot, D. Gingras, J. Camirand Lemyre, M. Pioro-Ladrière, and C. N. Allen, *Nano Lett.* **14**, 882 (2014).

[37] S. Kano, Y. Azuma, D. Tanaka, M. Sakamoto, T. Teranishi, L. W. Smith, C. G. Smith, and Y. Majima, *J. Appl. Phys.* **114**, 223717 (2013).

[38] Y. Yuzhelevski, M. Yuzhelevski, and G. Jung, *Rev. Sci. Instrum.* **71**, 1681 (2000).

[39] C. M. Chang, S. S. Chung, Y. S. Hsieh, L. W. Cheng, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, *Tech. Dig. Int. Electron Devices Meet. IEDM* 8 (2008).

[40] Z. Çelik-Butler, P. Vasina, and N. V. Amarasinghe, *IEEE Trans. Electron*

Devices **47**, 646 (2000).

[41] F. M. Puglisi, P. Pavan, D. Ingegneria, V. Vignolese, A. Padovani, L. Larcher, and V. Amendola, *Proc of IEEE ESSDERC*, 274 (2012).

[42] S. Choi, Y. Yang, and W. Lu, *Nanoscale* **6**, 400 (2014).

[43] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada, *IEEE Electron Device Lett.* **31**, 1302 (2010).

[44] Y. Vardi, A. Guttman, and I. Bar-Joseph, *Nano Lett*. **14**, 2794 (2014).

[45] A. J. Heeger, S. Kivelson, J. R. Schrieffer, and W. P. Su, *Rev. Mod. Phys*. **60**, 781 (1988).

[46] S. R. Forrest, *Nature* **428**, 911 (2004).

[47] M. Muccini, *Nat. Mater*. **5**, 605 (2006).

[48] A. L. Briseno, S. C. B. Mannsfeld, M. M. Ling, S. Liu, R. J. Tseng, C. Reese, M. E. Roberts, Y. Yang, F. Wudl, and Z. Bao, *Nature* **444**, 913 (2006).

[49] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, and A. Facchetti, *Nature* **457**, 679 (2009).

[50] T. Sekitani, H. Nakajima, H. Maeda, T. Fukushima, T. Aida, K. Hata, and T. Someya, *Nat. Mater.* **8**, 494 (2009).

[51] M. Segal, M. Singh, K. Rivoire, S. Difley, T. V. A. N. Voorhis, and M. A. Baldo, *Nat. Mater.* **6**, 2 (2007).

[52] G. Schwartz, B. C. Tee, J. Mei, A. L. Appleton, D. H. Kim, H. Wang, and Z. Bao, *Nat. Commun.* **4**, 1858 (2013).

[53] J. Ouyang, C. W. Chu, C. R. Szmanda, and L. Ma and Y. Yang, *Nat. Mater*. **3**, 918 (2004).

[54] Y. Yang, J. Ouyang, L. Ma, R. J. Tseng, and C. Chu, *Adv. Funct. Mater.* **16**, 1001 (2006).

[55] J. C. Scott and L. D. Bozano, *Adv. Mater*. **19**, 1452 (2007).

[56] Q. Ling, D. Liaw, C. Zhu, D. S. Chan, E. Kang, and K.-G. Neoh, *Prog. Polym. Sci*. **33**, 917 (2008).

[57] Y. Ji, D. F. Zeigler, D. S. Lee, H. Choi, A. K.-Y. Jen, H. C. Ko, and T.-W. Kim, *Nat. Commun*. **4**, 2707 (2013).

[58] L. D. Bozano, B. W. Kean, M. Beinhoff, K. R. Carter, P. M. Rice, and J. C. Scott, *Adv. Funct. Mater.* **15**, 1933 (2005).

[59] K. Asadi, M. Li, N. Stingelin, P. W. M. Blom, and D. M. De Leeuw, *Appl. Phys. Lett*. **97**, 193308 (2010).

[60] S. Song, B. Cho, T. Kim, Y. Ji, M. Jo, G. Wang, M. Choe, Y. H. Kahng, H. Hwang, and T. Lee, *Adv. Mater.* **22**, 5048 (2010).

[61] B. Cho, T. Kim, S. Song, Y. Ji, M. Jo, H. Hwang, G. Jung, and T. Lee, *Adv. Mater.* **22**, 1228 (2010).

[62] Y. Ji, B. Cho, S. Song, T. Kim, M. Choe, Y. H. Kahng, and T. Lee, *Adv. Mater.* **22**, 3071 (2010).

[63] S. Song, J. Jang, Y. Ji, S. Park, T. Kim, Y. Song, M. Yoon, H. Cho, G. Jung, and T. Lee, *Org. Electron.* **14**, 2087 (2013).

[64] J. J. Kim, B. Cho, K. S. Kim, T. Lee, and G. Y. Jung, *Adv. Mater.* **23**, 2104 (2011).

[65] J. E. Green, J. Wook Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. DeIonno, Y. Luo, B. a Sheriff, K. Xu, Y. Shik Shin, H.-R. Tseng, J. F. Stoddart, and J. R. Heath, *Nature* **445**, 414 (2007).

[66] A. A. Zakhidov, J. Lee, J. A. Defranco, H. Fong, P. G. Taylor, M. Chatzichristidi, K. Ober, and G. G. Malliaras, *Chem. Sci.* **2**, 1178 (2011).

[67] C. Y. Ouyang, J. Lee, M. E. Krysak,, J. Sha, and C. K. Ober, *J. Mater. Chem.* **57** 5746 (2012).

[68] J. Park, W. Nam, S. Seo, Y. Kim, Y. Oh, G. Lee, and U. Paik, *Nano lett.* **9**, 1713 (2009).

[69] G. Yang, H.-Y. Chen, L. Ma, Y. Shao, and Y. Yang, *Appl. Phys. Lett.* **95**, 203506 (2009).

[70] J. Lee, M. Jo, D. J. Seong, J. Shin, and H. Hwang, *Microelectron. Eng.* **88**, 1113 (2011).

[71] C. J. Amsinck, N. H. Di Spigna, D. P. Nackashi, and P. D. Franzon, *Nanotechnology* **16**, 2251 (2005).

[72] D. Y. Yun, W. S. Song, T. W. Kim, S. W. Kim, S. W. Kim, D. Y. Yun, W. S. Song, T. W. Kim, and W. Kim, *Appl. Phys. Lett.* **101**, 103305, (2012).

[73] Y. Ji, S. Lee, B. Cho, S. Song, and T. Lee, *ACS Nano* **5**, 5995 (2011).

[74] D.-I. S. and J.-H. K. and D.-H. P. and W. K. C. and F. L. and J. H. H. and T. W. Kim, *Nanotechnology* **19**, 55204 (2008).

[75] B. Cho, J. M. Yun, S. Song, Y. Ji, D. Y. Kim, and T. Lee, *Adv. Funct. Mater.* **21**, 3976 (2011).

[76] Y. Song, J. Jang, D. Yoo, S. H. Jung, S. Hong, J. K. Lee, and T. Lee, *Org. Electron. Physics, Mater. Appl.* **17**, 192 (2015).

[77] L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott, *Appl. Phys. Lett.* **84**, 607 (2004).

[78] J. Rivnay, L. H. Jimison, J. E. Northrup, M. F. Toney, R. Noriega, S. Lu, T.

J. Marks, A. Facchetti, and A. Salleo, *Nat. Mater.* **8**, 952 (2009).

[79] Y. Zhou, C. Fuentes-Hernandez, J. Shim, J. Meyer, A. J. Giordano, H. Li, P. Winget, T. Papadopoulos, H. Cheun, J. Kim, M. Fenoll, A. Dindar, W. Haske, E. Najafabadi, T. M. Khan, H. Sojoudi, S. Barlow, S. Graham, J.-L. Bredas, S. R. Marder, A. Kahn, and B. Kippelen, *Science* **336**, 327 (2012).

[80] M. J. Rozenberg, I. H. Inoue, and M. J. Sanchez, *Phys. Rev. Lett.* **92**, 178302 (2004).

[81] K. Asadi, D. M. de Leeuw, B. de Boer, and P. W. M. Blom, *Nat. Mater.* **7**, 547 (2008).

[82] W. Tang, H. Z. Shi, G. Xu, B. S. Ong, Z. D. Popovic, J. C. Deng, J. Zhao, and G. H. Rao, *Adv. Mater.* **17**, 2307 (2005).

[83] N. Kang, B. Cho, B. Kang, S. Song, T. Lee, and J. Lee, *Adv. Mater.* **24**, 385 (2012).

[84] F. Verbakel, S. C. J. Meskers, R. A. J. Janssen, H. L. Gomes, M. Cölle, M. Büchel, and D. M. De Leeuw, *Appl. Phys. Lett.* **91,** 192103 (2007).

[85] S. B. Lee, S. Park, J. S. Lee, S. C. Chae, S. H. Chang, M. H. Jung, Y. Jo, B. Kahng, B. S. Kang, M. J. Lee, and T. W. Noh, *Appl. Phys. Lett.* **95**, 7 (2009).

[86] P. R. F. Rocha, H. L. Gomes, L. K. J. Vandamme, Q. Chen, A. Kiazadeh, D. M. De Leeuw, and S. C. J. Meskers, *IEEE Trans. Electron Devices* **59**, 2483 (2012).

[87] A. Carbone, B. K. Kotowska, and D. Kotowski, *Phys. Rev. Lett.* **95**, 236601 (2005).

[88] N. Clément, S. Pleutin, O. Seitz, S. Lenfant, and D. Vuillaume, *Phys. Rev.*

B **76**, 205407 (2007).

[89] Y. Kim, H. Song, D. Kim, T. Lee, and H. Jeong, *ACS Nano* **4**, 4426 (2010).

[90] J. V. Mantese and W. W. Webb, *Phys. Rev. Lett.* **55**, 2212 (1985).

[91] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, *Nat. Nanotechnol.* **5**, 148 (2010).

[92] A. D. Yu, T. Kurosawa, Y. H. Chou, K. Aoyagi, Y. Shoji, T. Higashihara, M. Ueda, C. L. Liu, and W. C. Chen, *ACS Appl. Mater. Interfaces* **5**, 4921 (2013).

[93] S. K. Hwang, J. M. Lee, S. Kim, J. S. Park, H. Il Park, C. W. Ahn, K. J. Lee, T. Lee, and S. O. Kim, *Nano Lett.* **12**, 2217 (2012).

[94] H. T. Lin, Z. Pei, and Y. J. Chan, *IEEE Electron Device Lett.* **28**, 569 (2007).

[95] S. Nau, S. Sax, and E. J. W. List-Kratochvil, *Adv. Mater.* **26**, 2508 (2014).

[96] J. K. Lee, S. Jung, J. Park, S. W. Chung, J. Sung Roh, S. J. Hong, I. Hwan Cho, H. I. Kwon, C. Hyeong Park, B. G. Park, and J. H. Lee, *Appl. Phys. Lett.* **101**, (2012).

[97] S. M. Islam, P. Banerji, and S. Banerjee, *Org. Electron.* **15**, 144 (2014).

[98] J.-C. Chen, C.-L. Liu, Y.-S. Sun, S.-H. Tung, and W.-C. Chen, *Soft Matter* **8**, 526 (2012).

[99] D. I. Son, C. H. You, J. H. Jung, and T. W. Kim, *Appl. Phys. Lett.* **97**, 013304 (2010).

[100] T. W. Kim, Y. Yang, F. Li, and W. L. Kwan, *NPG Asia Mater.* **4**, e18 (2012).

[101] A. Carbone, B. K. Kotowska, and D. Kotowski, *Phys. Rev. Lett.* **95**, 236601 (2005).

[102] J. Lee, H. Y. Jeong, I. Cho, J. Y. Lee, S. Choi, H. Kwon, and J. Lee, *IEEE Electron Device Lett.* **31**, 603 (2010).

[103] L. K. J. Vandamme and M. Macucci, *AIP Conf. Proc.* **800**, 436 (2005).

[104] J. Planès and A. François, Phys. Rev. B **70**, 184203 (2004).

[105] D. A. Rudman, J. J. Calabrese, and J. C. Garland, *Phys. Rev. B*. 33, 1456 (1986).

[106] A. J. Breeze, S. A. Carter, G. B. Alers, and M. B. Heaney, *Appl. Phys. Lett.* **76**, 592 (2000).

[107] R. De Sousa, K. B. Whaley, F. K. Wilhelm, and J. Von Delft, *Phys. Rev. Lett.* **95**, 247006 (2005).

[108] A. Carbone, C. Pennetta, and L. Reggiani, *Appl. Phys. Lett.* **95**, 233303 (2009).

[109] J. Wu, L. Ma, and Y. Yang, *Phys. Rev. B* **69**, 115321 (2004).

[110] W. Graupner, G. Leditzky, G. Leising, and U. Scherf, *Phys. Rev. B* **54**, 7610 (1996).

[111] D. A. Buchanan, M. V Fischetti, and D. J. Dimaria, *Phys. Rev. B* **43**, 1471 (1991).

[112] K. Takizawa, S. Asai, and S. Ando, *Polym. J.* **46**, 201 (2014).

[113] M. Meunier, N. Quirke, and A. Aslanides, *J. Chem. Phys.* **115**, 2876 (2001).

[114] B. C.-K. Tee, A. Chortos, A. Berndt, A. K. Nguyen, A. Tom, A. McGuire, Z. C. Lin, K. Tien, W.-G. Bae, H. Wang, P. Mei, H.-H. Chou, B. Cui, K.

Deisseroth, T. N. Ng, and Z. Bao, *Science* **350**, 313 (2015).

[115] J. You, L. Dou, K. Yoshimura, T. Kato, K. Ohya, T. Moriarty, K. Emery, C.-C. Chen, J. Gao, G. Li, and Y. Yang, *Nat. Commun.* **4**, 1446 (2013).

[116] Y. Zhao, C. A. Di, X. Gao, Y. Hu, Y. Guo, L. Zhang, Y. Liu, J. Wang, W. Hu, and D. Zhu, *Adv. Mater.* **23**, 2448 (2011).

[117] S. Savagatrup, E. Chan, S. M. Renteria-Garcia, A. D. Printz, A. V. Zaretski, T. F. O'Connor, D. Rodriquez, E. Valle, and D. J. Lipomi, *Adv. Funct. Mater.* **25**, 427 (2015).

[118] T. W. Kim, D. F. Zeigler, O. Acton, H. L. Yip, H. Ma, and A. K. Y. Jen, *Adv. Mater.* **24**, 828 (2012).

[119] G. Khurana, P. Misra, and R. S. Katiyar, *Carbon* **76**, 341 (2014).

[120] Y. Song, H. Jeong, J. Jang, T.-Y. Kim, D. Yoo, Y. Kim, H. Jeong, and T. Lee, *ACS Nano* **9**, 7697 (2015).

[121] A. Laiho, H. S. Majumdar, J. K. Baral, F. Jansson, R. Österbacka, O. Ikkala, A. Laiho, H. S. Majumdar, J. K. Baral, and F. Jansson, *Appl. Phys. Lett.* **93,** 203309 (2008).

[122] B. Fourcade and A.-M. S. Tremblay, *Phys. Rev. B* **34**, 7802 (1986).

[123] A. A. Balandin, *Nat. Nanotechnol*. **8**, 549 (2013).

[124] L. K. J. Vandamme, X. Li, and D. Rigaud, *IEEE Trans. Electron Devices* **41**, 1936 (1994).

[125] J. C. Ashley and M. W. Williams, *Radiat. Res.* **81**, 364 (1980).

[126] S. M. Rossnagel and T. S. Kuan, *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **22**, 240 (2004).

[127] S.-M. Joe, J.-H. Yi, S.-K. Park, H. Shin, B.-G. Park, Y. J. Park, and J.-H.

Lee, *IEEE Trans. Electron Devices* **58**, 67 (2011).

[128] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, and Y. Hayashi, *IEDM Tech. Dig.* 759 (2009).

[129] S. M. Yu, X. M. Guan, and H. S. P. Wong, *Appl. Phys. Lett.* **99**, 63507 (2011).

국문초록

유기저항변화 메모리에 대한 4K-비트 마이크로 스케일 고집적화와 전기 노이즈 분석

유기 저항변화메모리는 좋은 안정성, 동작성, 유연성, 그리고 용액 공정이 가능하다는 장점이 있기에 연구자들에게 지대한 관심을 받아왔다. 이러한 장점들을 이용하여, 본 연구 그룹에서는 1D-1R 유기 메모리, 수직 집적 구조 메모리, 유연한 유기 메모리 등 유기 메모리에 대한 다양한 소자 구조 개발을 해왔다. 하지만, 유기 메모리의 고집적화는 실현되기 어려운 문제점이 있었는데 그 이유는 아세톤과 같은 유기 용매를 사용하는 상용 광식각 방법을 유기 메모리 제작에 적용할 수 없었기 때문이다. 또한 고분자의 매우 무질서한 정렬 상태와 유기물 혼합물의 비균질성 때문에 유기 저항 변화 메모리의 저항변화 원리와 전하 수송 원리 등은 잘 안 알려져 있다. 이러한 맥락에서 본 학위 논문에서는 불소화 화합물 기반의 광식각 방법을 이용한 유기메모리의 고집적화와 노이즈 분석을 통한 유기 메모리의 저항변화 원리와 전하 수송 원리에 대한 고찰을 다루고 있다.

먼저, 유기 저항 변화메모리 (PI:PCBM) 에 대한 불소화 화합물 광식각 방법을 이용해 4k-bit의 유기 소자를 4 mm^2 의 작은 면적에 집적할 수 있었다. 완성된 소자는 손상을 입지 않은 채로 좋은 메모리 특성을 보였다. 또한 80 % 정도의 수율을 보여 통계적으로도 광식각 과정을 통해 손상을 거의 입지 않은 것을 확인하였다. 더 나아가 유연성 기판 위에서 같은 방법으로 유기 메모리를 제작 및 집적하여 다양한 기술 응용의 가능성을 보여주었다.

그리고 유기 나노 혼합물 저항 변화 메모리 물질인 PI:PCBM과 PS:PCBM의 노이즈 특성을 연구한 결과를 기술하였다. 여러 중간 저항상태와 음의 미분저항이 나오는 전압영역에서의 전류 노이즈를 측정하였다. 전류 노이즈에서 관측된 1/f 타입의 노이즈를 분석한 결과 스며듦 현상과 관련하여 노이즈와 저항 사이의 멱급수 관계를 확인하였다. 간단한 선형 관계식으로 전하 덫에서의 전하 잡힘-풀림을 고려하여 스며듦 현상과 음의 미분저항이 인가전압에 의한 전도상 비율 조절로 이해될 수 있다는 것을 밝혔다. 또한 추가 온도 변화실험을 통하여 노이즈와 저항 사이의 멱급수 관계와 음의 미분저항에서의 텔레그래픽 노이즈의 변화를 관찰하고 분석하였다. 이를 통하여 각 중간 저항 상태는 유기 나노 혼합물 층 내에서 전하 덫으로 이뤄진 국소적인 전류경로로 표현될 수 있으며, 이는 깊은 전하 덫에서 전하가 열 적 여기를 통해 갇히고 빠져나가는 현상에서 기인함을 보여주었다.

Keywords : 유기 저항변화 메모리, 직교광식각 방법, 1/f 노이즈, 랜덤 텔레그래프 노이즈, 스며듦 현상
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